The CubeSat Kit Hinge™ System
&
Designing your own CSK PPM

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Outline

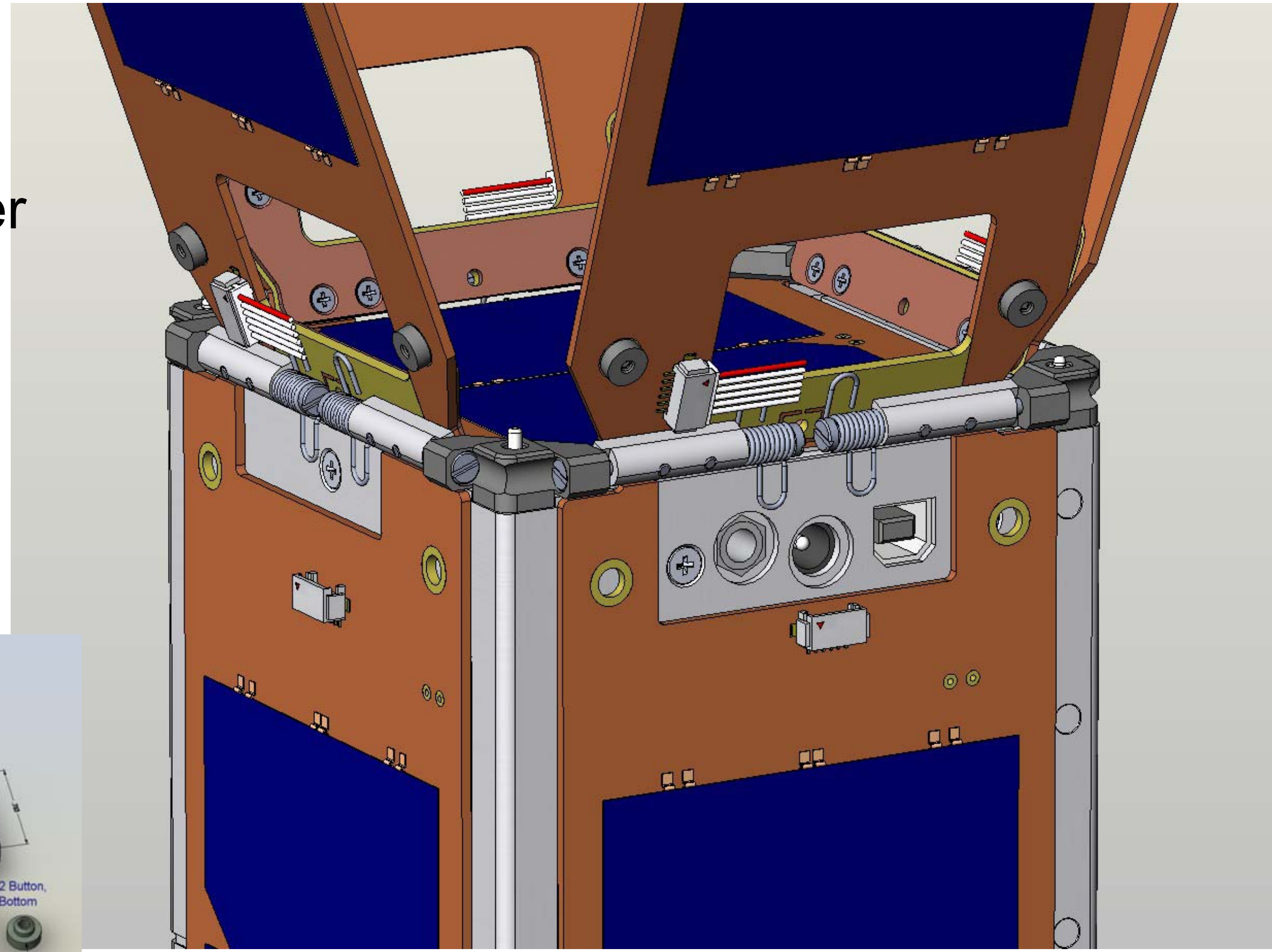
- Part I: The CubeSat Kit Hinge System
- Part II: Design your own CubeSat Kit Pluggable Processor Module (PPM)

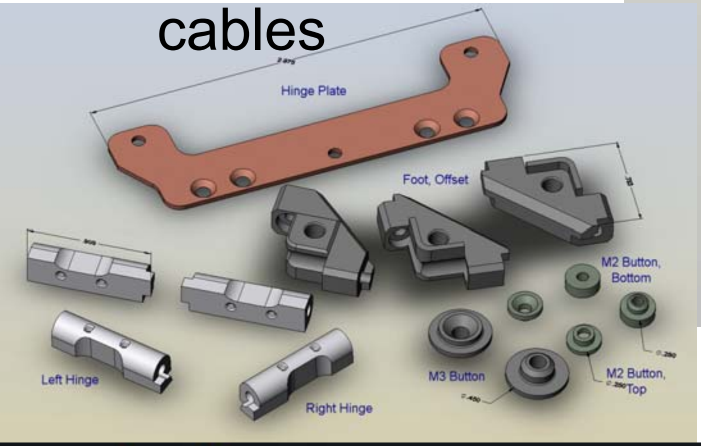
I: The CSK Hinge System

Feature / Characteristic	Requirements
Structure compatibility	CubeSat Kit Rev D and later (0.5U, 1U, 1.5U, 2U & 3U)
Number of panels supported	Up to eight (I.e., up to four on each end)
Solar cell surfaces supported	Fixed side panels & single- or double-sided deployable panels
Minimum panel mass supported	150g per deployable panel
End bias	None – panels can be hinged on either end of CubeSat Kit
Harness compatibility	six 26AWG wires per deployable panel
Number of actuations	> 100
CDS compatibility	Must fit within P-POD (I.e., max 6.5mm normal height)
Additional mass	< 75g for four deployable panels, all hinged on one end
Volume	Located entirely “outside” 100mm x 100mm cross-section
Deployment angles	0 to 190 degrees per panel
Deployment (spring) forces	Sufficient to open fully in zero-g vacuum environment
Material(s)	Hard-anodized aluminum, stainless steel
Testing regime	Protoflight standards
Vibration compatibility	NASA GEVS GSFC-STD-7000
Vacuum compatibility	10^{-4} Torr
Operating temperature range	-100C to +100C

CSK Hinge Components

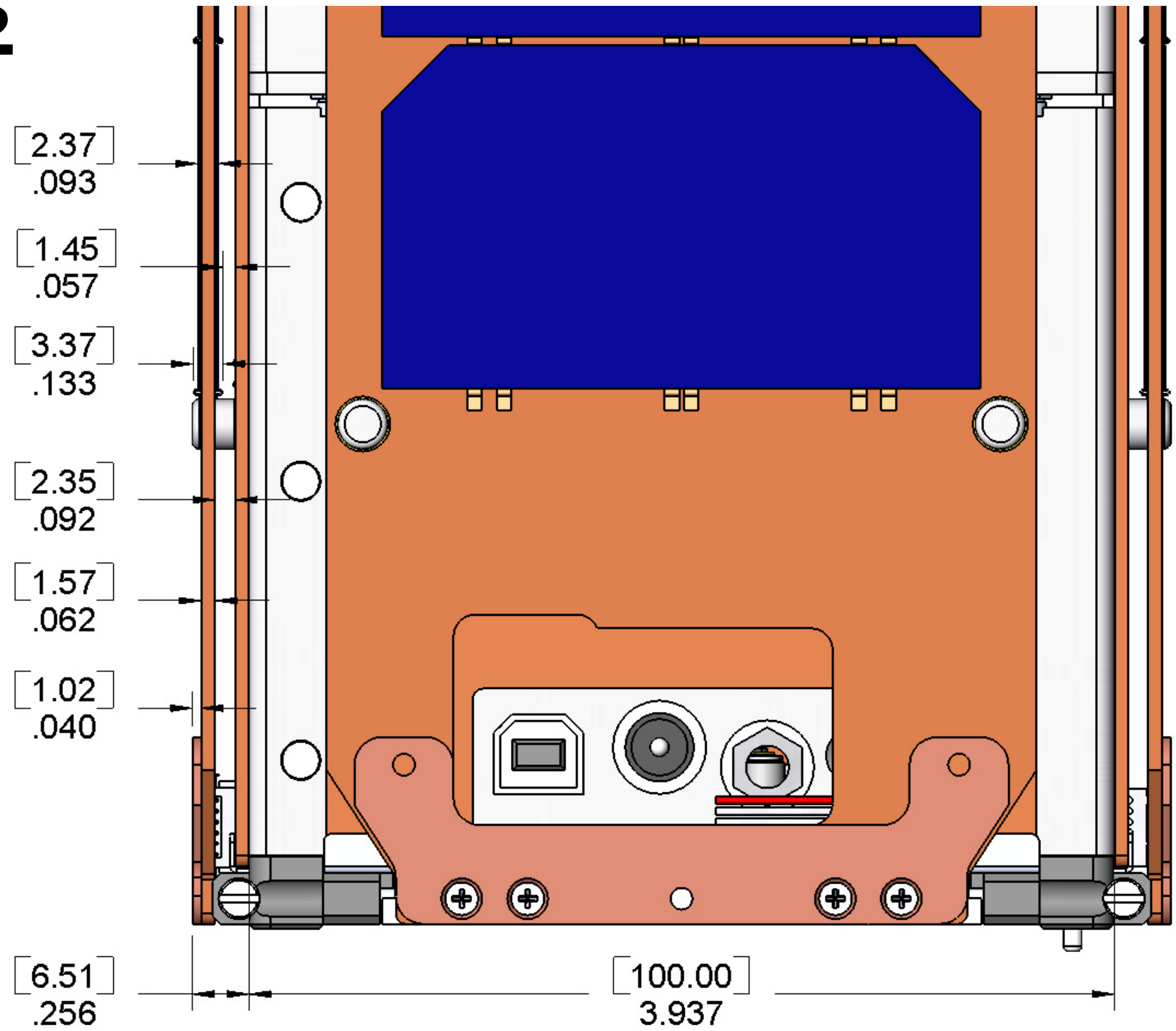
- Hinge feet & hinges
- Precision shoulder bolts
- Springs
- Large & small buttons
- Harnesses & cables





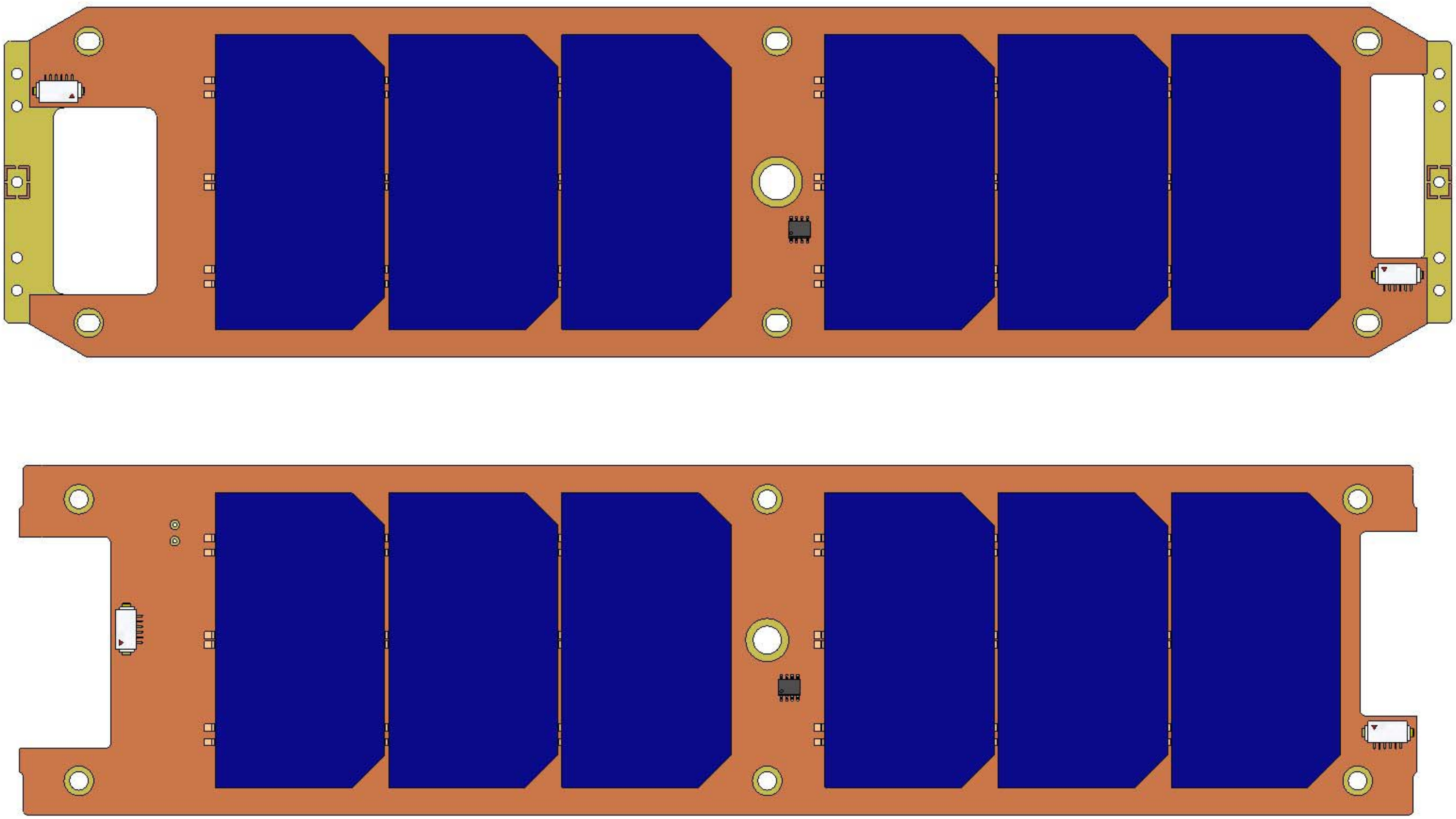
Panel Details

- 1.6mm (0.062”) PCBs leave precious little room for solar cells on 3 available faces
- Buttons protect facing cells from potentially damaging contact, align panels, relieve stress on hinges, and perform other functions

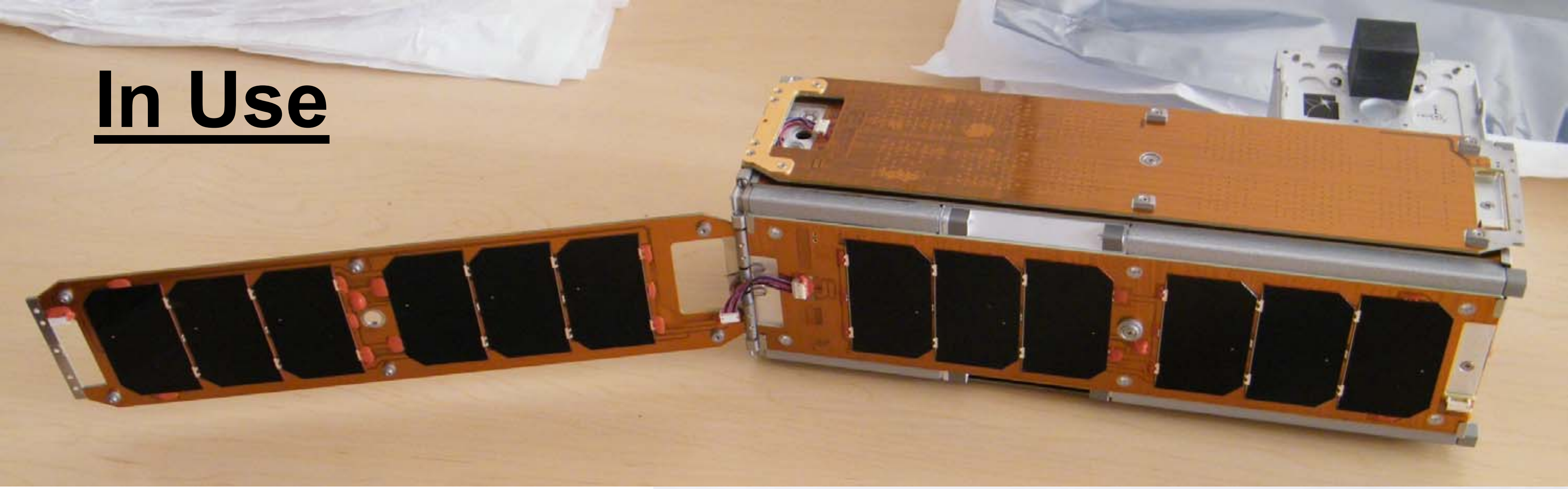


Panel Designs

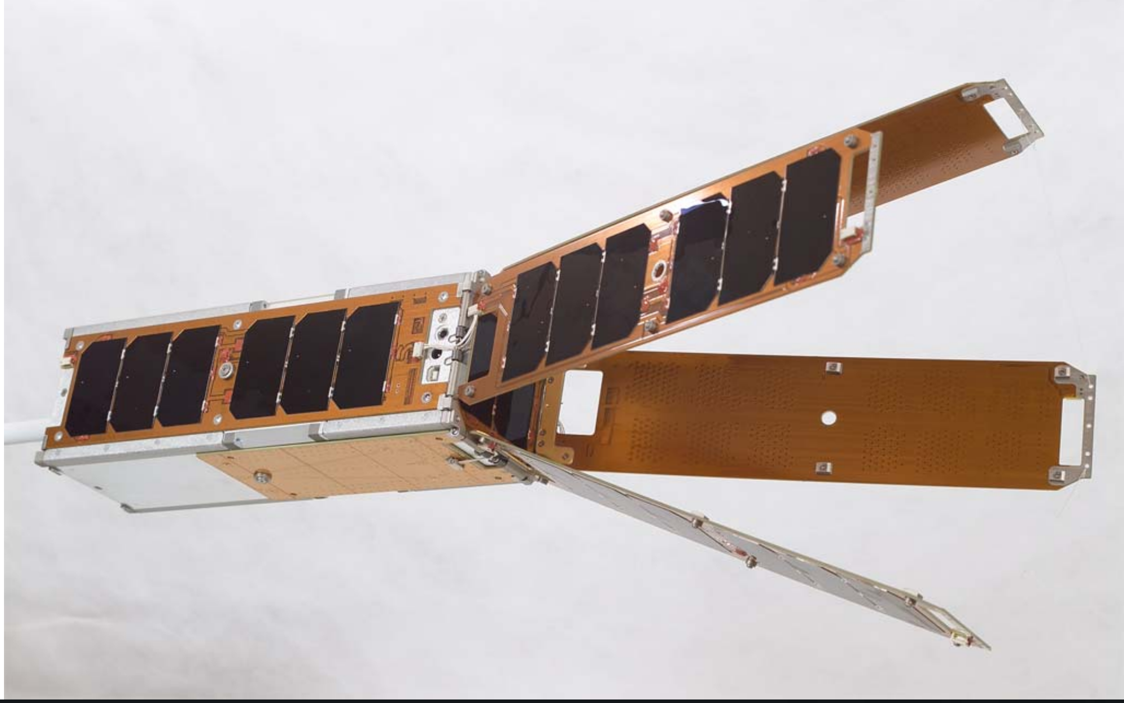
- Panels are “build to print”
- Deployable panels can be hinged on either end



In Use

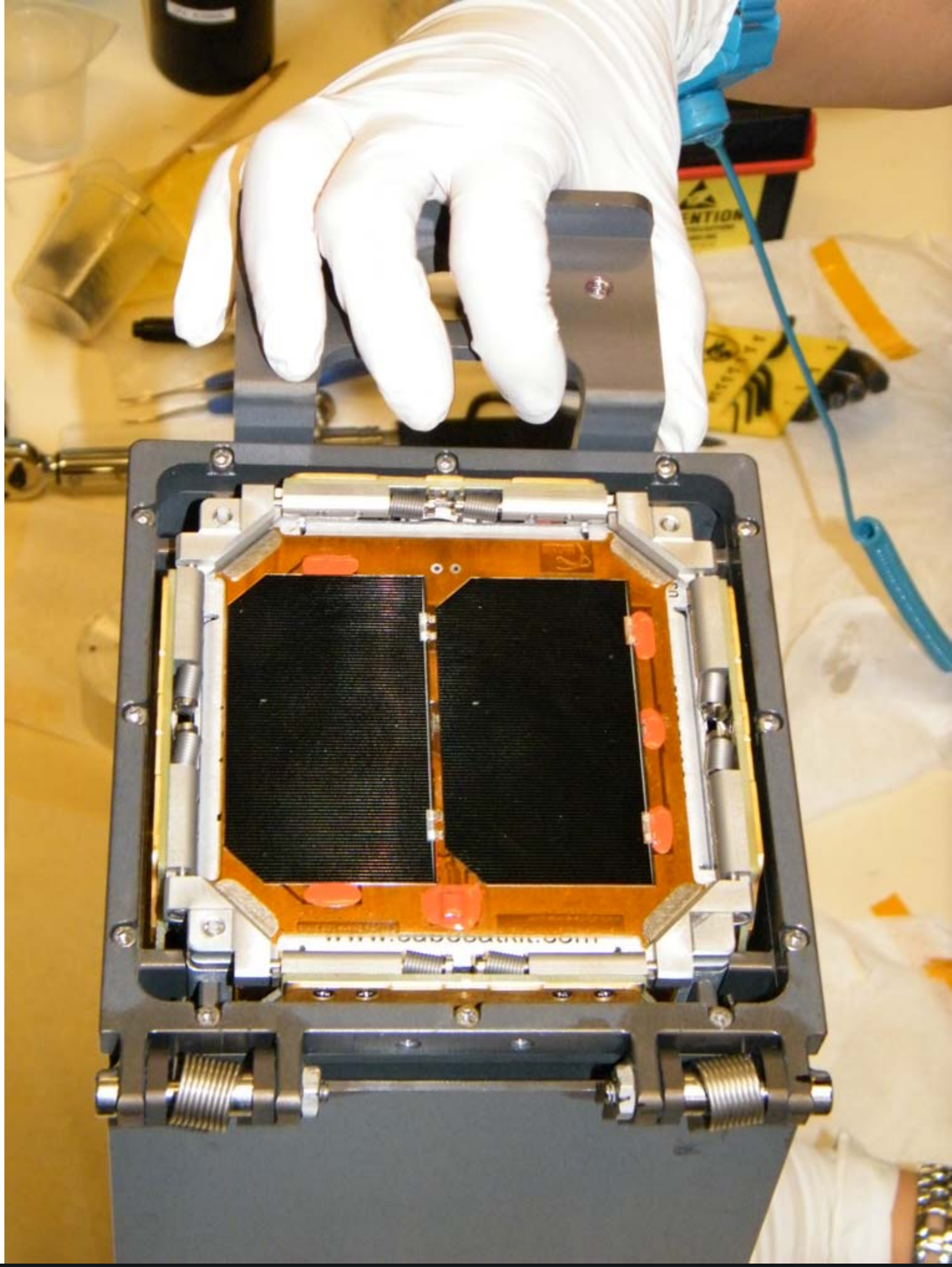


- Pumpkin's MISC 2 is the first CubeSat to utilize the CubeSat Kit Hinge
- All four single-sided deployable panels are hinged at bus end



Vibe Testing

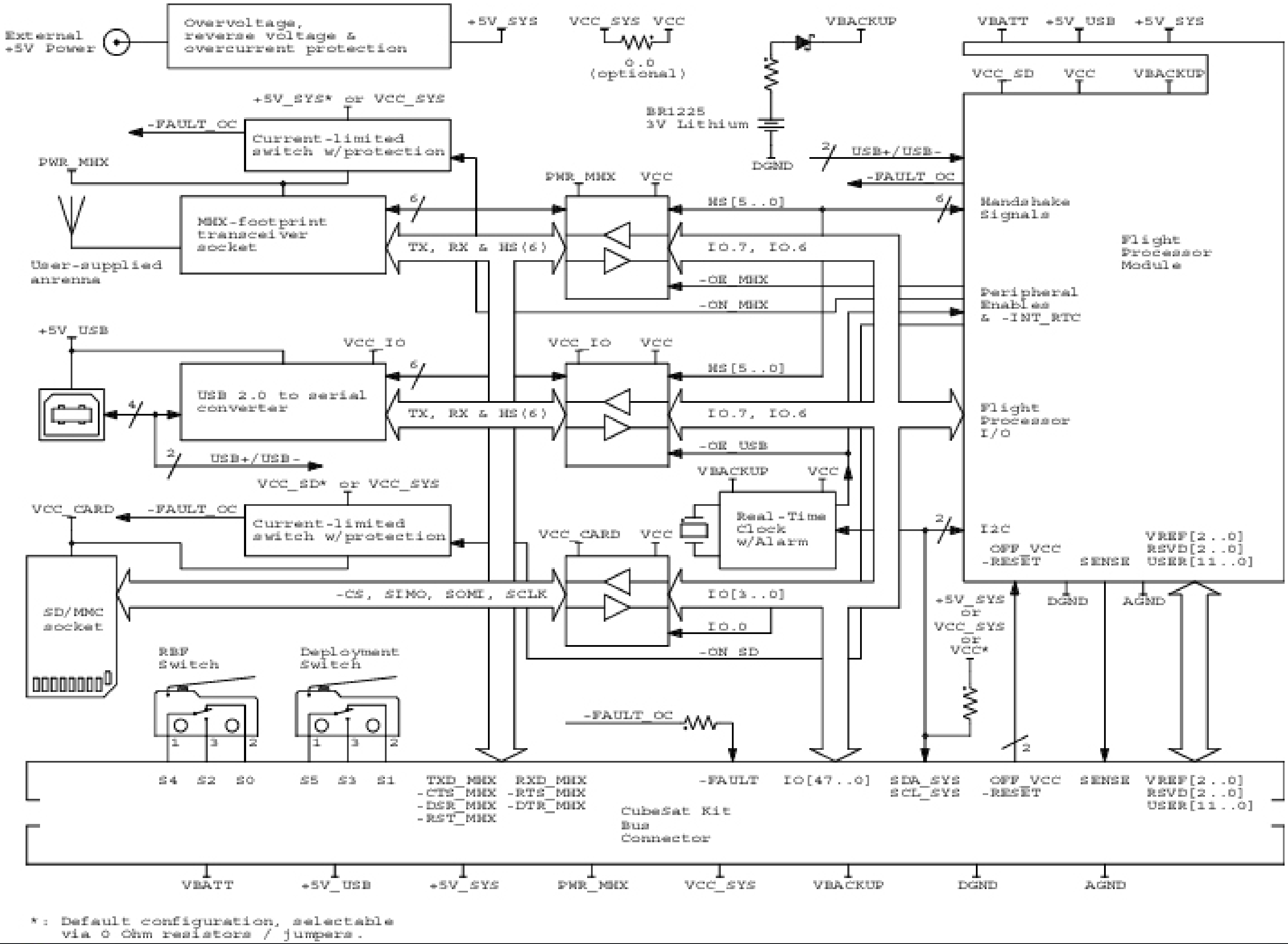
- MISC 2 in a P-POD at Cal Poly in March 2009
- A close fit!
- Two MISC 2s were tested – no anomalies



II: Design your own CSK PPM

- Pluggable Processor Modules (PPMs) enable rapid adaptation of the CubeSat Kit architecture to an existing codebase that has tight ties to a particular processor architecture or family.
- The PPM:
  - is where your CubeSat's processor(s) is(are) located
  - takes power from the CSK bus, uses it locally, conditions it for the Motherboard (MB) and optionally for the CSK bus
  - accepts a few high-level control signals from the CSK bus
  - connects to various resources on the MB
  - connects to I/O and other signals on the CSK bus

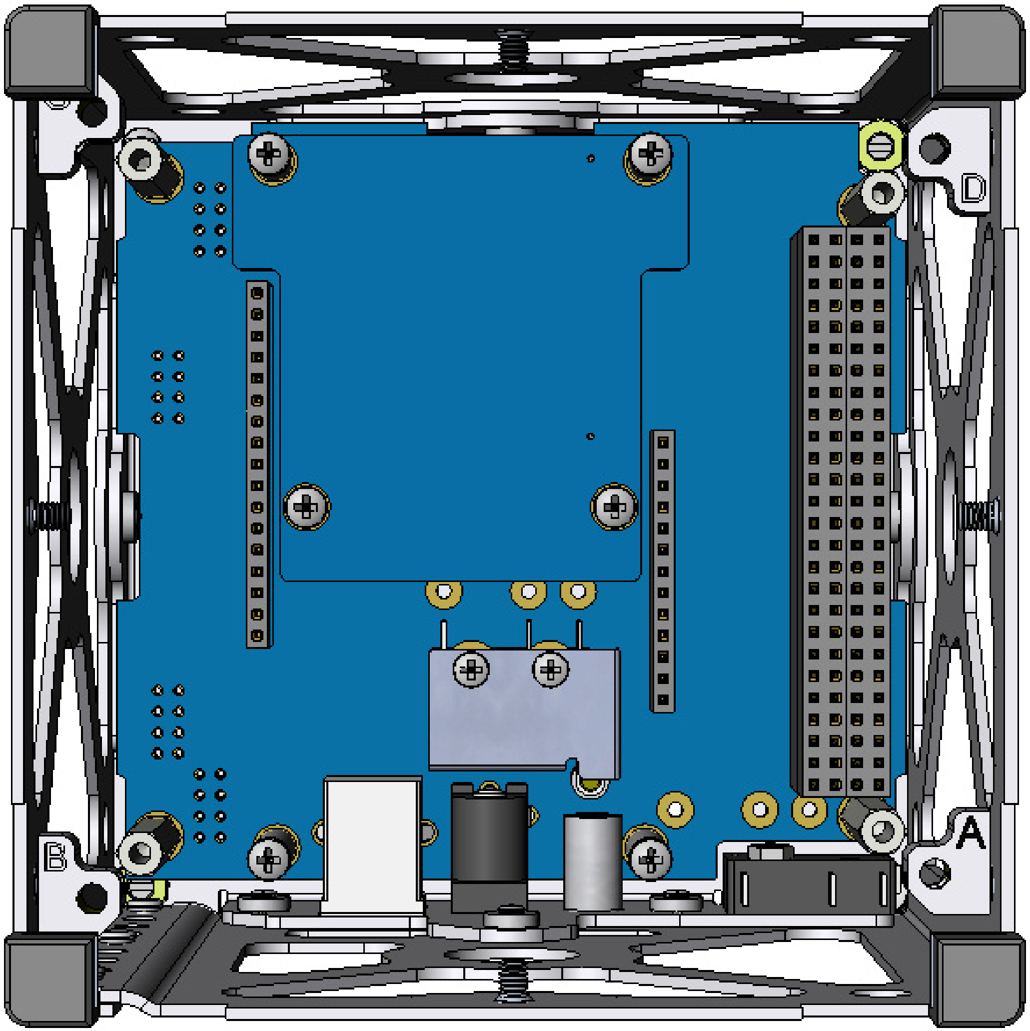
CSK Architecture Block Diagram



PPM Provides Flexibility

- As a PPM designer, you have the freedom to specify:
  - which processor(s) to use
  - which voltage(s) to operate at
  - which clock sources to use
  - which additional external components (e.g., external memory, WDTs, user debug connectors) to use
  - PCB details (e.g., how many layers, material)
  - etc.

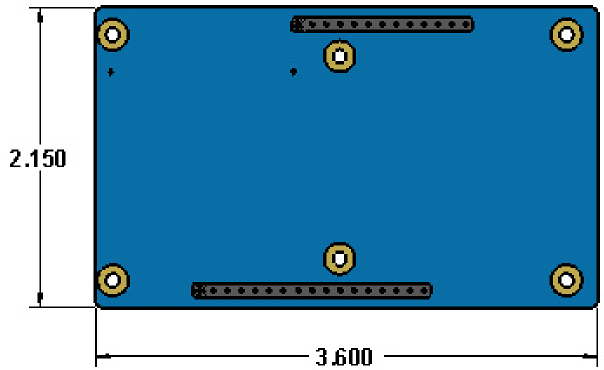
PPM on MB – Top View

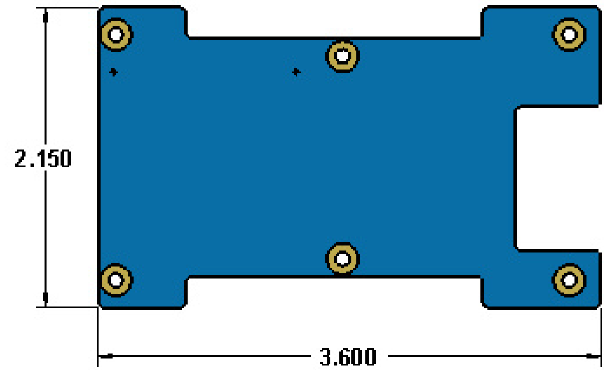


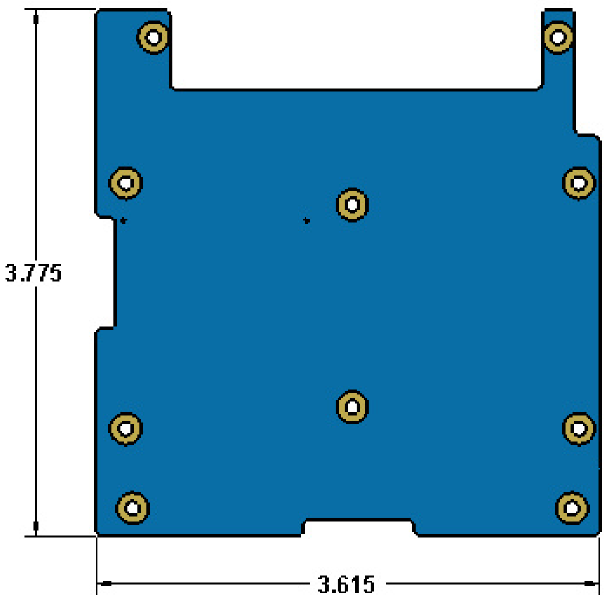
PPM A1/A2/A3

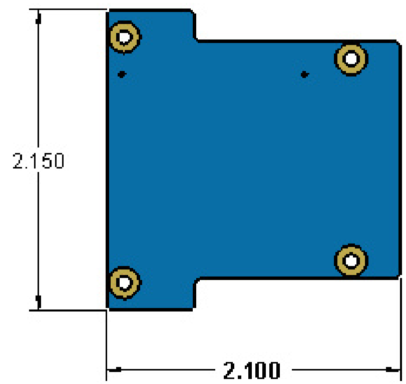
Top view of Pluggable Processor Module (PPM) mounted on Motherboard (MB) inside 1U skeletonized CubeSat Kit.

Allowable PPM PCB Sizes



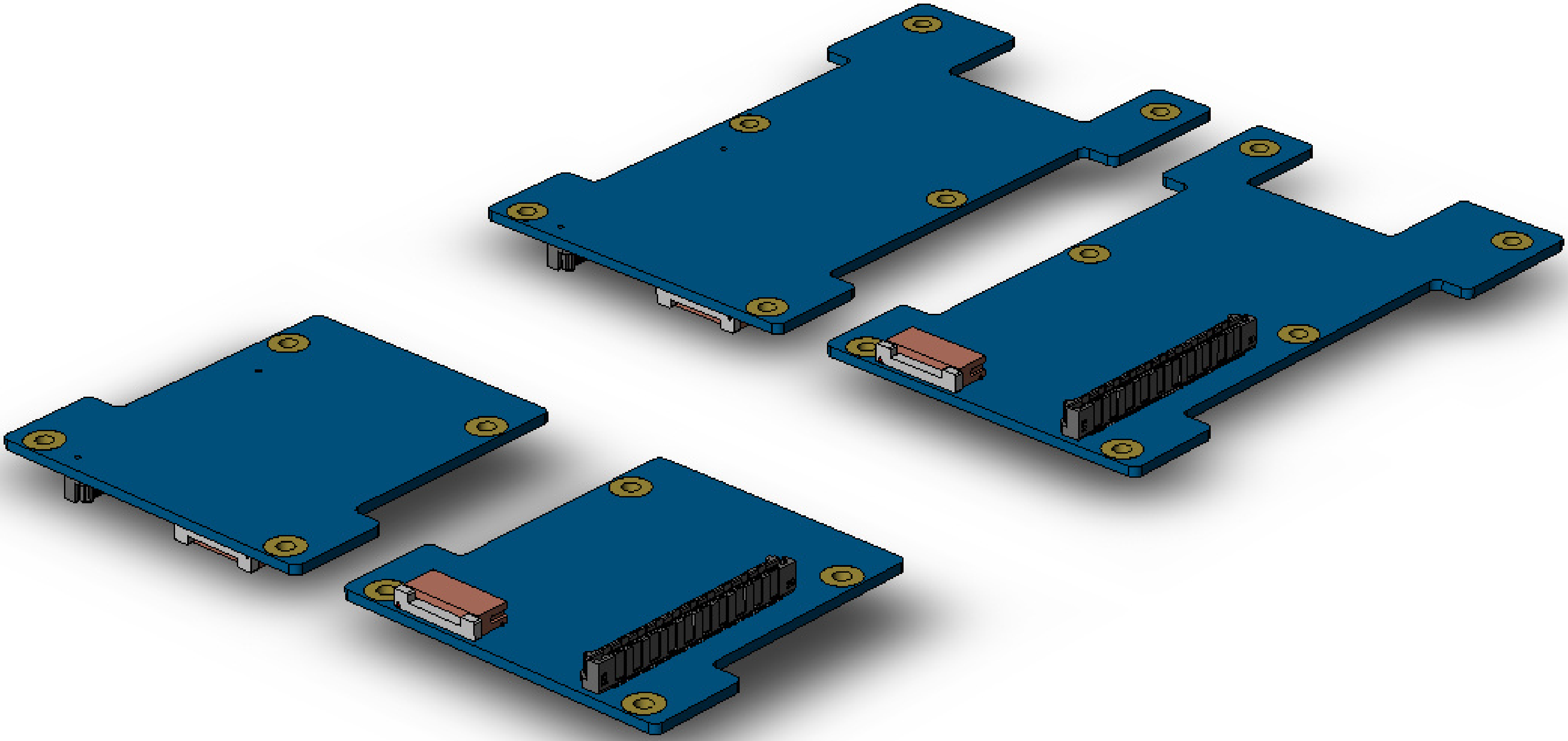






Examples of CubeSat Kit Pluggable Processor Module (PPM) PCB outlines. Dimensions in inches.

PPM PCB Views



Top and bottom views of bare example CubeSat Kit Pluggable Processor Module (PPM) PCBs.

Left/bottom: PPM A1/A2/A3 Right/top: PPM B1

PPM Connector Pinout

To/From Flight MCU on Processor Module

H10
LSS-150-02-L-DV

<->	IO.23	1	2	IO.47	<->
<->	IO.22	3	4	IO.46	<->
<->	IO.21	5	6	IO.45	<->
<->	IO.20	7	8	IO.44	<->
<->	IO.19	9	10	IO.43	<->
<->	IO.18	11	12	IO.42	<->
<->	IO.17	13	14	IO.41	<->
<->	IO.16	15	16	IO.40	<->
<->	IO.15	17	18	IO.39	<->
<->	IO.14	19	20	IO.38	<->
<->	IO.13	21	22	IO.37	<->
<->	IO.12	23	24	IO.36	<->
<->	IO.11	25	26	IO.35	<->
<->	IO.10	27	28	IO.34	<->
<->	IO.9	29	30	IO.33	<->
<->	IO.8	31	32	IO.32	<->
<->	IO.7 *	33	34	IO.31	<->
<->	IO.6 *	35	36	IO.30	<->
<->	IO.5	37	38	IO.29	<->
<->	IO.4	39	40	IO.28	<->
<->	IO.3 *	41	42	IO.27	<->
<->	IO.2 *	43	44	IO.26	<->
<->	IO.1 *	45	46	IO.25	<->
<->	IO.0 *	47	48	IO.24	<->
	+5V_USB	49	50	+5V_USB	
	+5V_SYS	51	52	+5V_SYS	
	VCC_SD	53	54	VCC_SD	
	VCC	55	56	VCC	
	DGND	57	58	DGND	
	AGND	59	60	AGND	
	VBATT	61	62	VBATT	
	VBACKUP	63	64	VBACKUP	
	VREF0	65	66	-FAULT_OC	-->
	VREF1	67	68	SENSE	-->
	VREF2	69	70	-RESET	<--
	RSVD0	71	72	OFF_VCC	<--
	RSVD1	73	74	SDA_SYS	<->
	RSVD2	75	76	SCL_SYS	-->
-->	USBDP/CB4	77	78	USER0	
-->	USBDM/CB2	79	80	USER1	
<--	-ON_SD	81	82	USER2	
<--	-ON_MHX	83	84	USER3	
<--	-OE_MHX	85	86	USER4	
<->	-OE_USB/-INT	87	88	USER5	
-->	HS0	89	90	USER6	
-->	HS1	91	92	USER7	
-->	HS2	93	94	USER8	
<--	HS3	95	96	USER9	
<--	HS4	97	98	USER10	
<--	HS5	99	100	USER11	

CubeSat Kit PPM connector on MB.

40 of 48 I/O pins are unallocated and always available to the user.

On-board peripherals have dedicated control signals (e.g., handshake signals HS[5..0], -ON_SD, etc.).

Entire CubeSat Kit Bus connector (except for S[5..0] & MHX socket signals) is available to PPM.

PPM Standardized Signals

- IO.[7..0]:
  - IO.[3..0]: SPI MISO/MOSI/SCLK & -CS_SD
  - IO.[5,4]: UART0
  - IO.[7,6]: UART1
- SCL_SYS, SDA_SYS: System I2C
- -FAULT_OC, SENSE: Power-related (optional)
- -RESET, OFF_VCC: Reset / power control
- -ON_SD: SD card power
- -OE_USB: USB interface
- -ON_MHX, -OE_MHX: MHX interface (optional)
- HS[5..0]: MHX/USB handshake signals (optional)
- VREF[2..0]: Reference voltages
- USBDP, USBDM: USB direct signals

PPM User Signals & Power

- PPM user signals
  - IO.[47..8] – as yet undefined, up to designer's discretion
  - USER[11..0] – undefined
- PPM power
  - +5V_USB & +5V_SYS: from EPS & USB to PPM
  - VCC_SD: from PPM to MB SD Card, +3.3V
  - VCC: on PPM, and to MB – can range from +2.7V to +5V
  - DGND: Digital ground
  - AGND: Analog (quiet) ground
  - VBATT: Raw battery voltage (e.g. +7.4V)
  - VBACKUP: +3V battery backup (e.g. for SRAM)

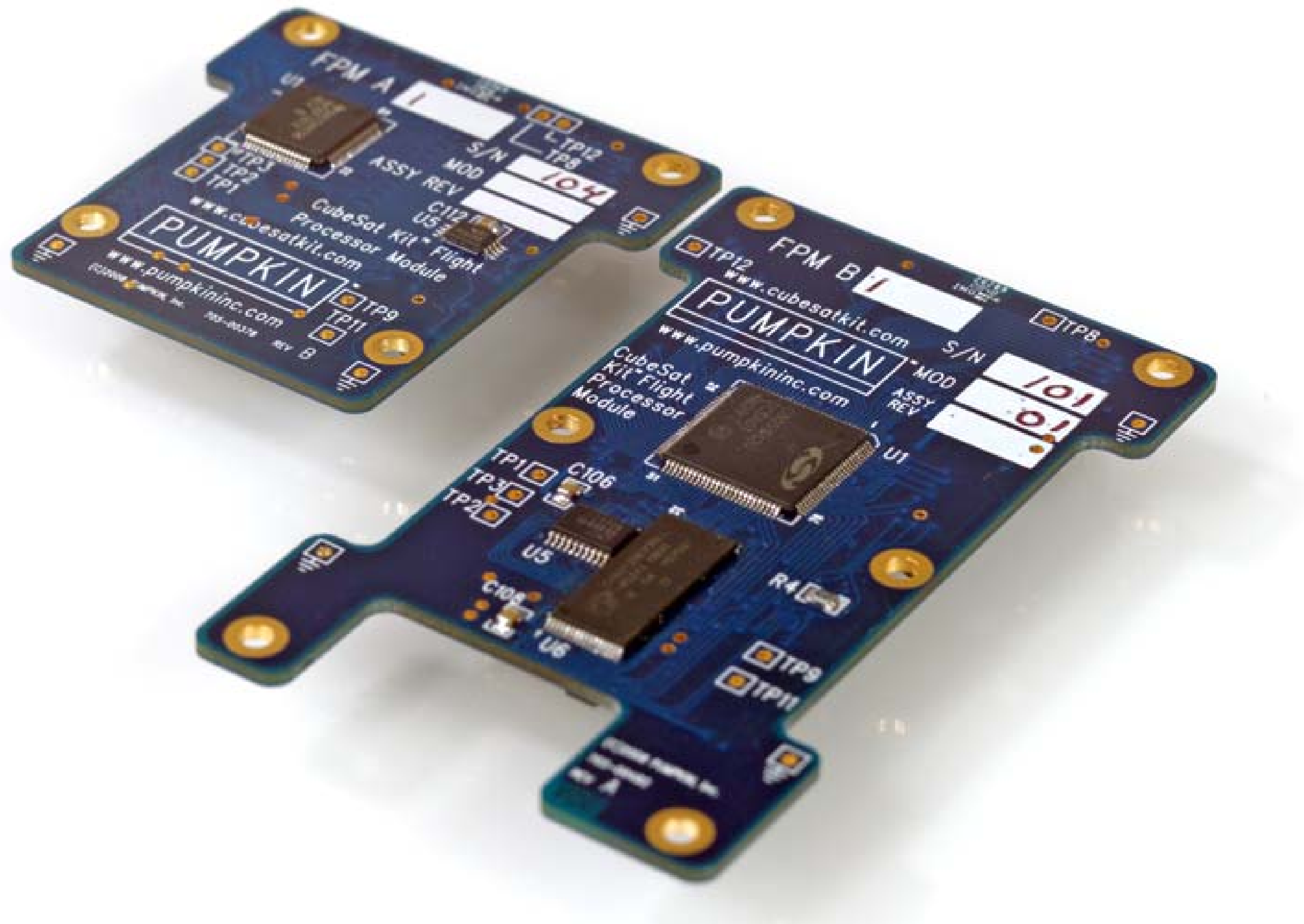
PPM A1: MSP430F1612

- Utilizes TI's MSP430F1612IPM (64-pin LQFP package)
- Regulates +5V_SYS & +5V_USB down to +3.3V for processor, VCC on MB and SD Card
- Has local POR supervisor & overcurrent protection / auto-reset
- Has 32.768kHz & 7.3728MHz crystals
- All 48 I/O pins to IO.[47..0] on CSK bus
- PCA9515 I2C isolator routes MSP430 SCL & SDA to SCL_SYS & SDA_SYS, enabled via –CS_SD
- Some I/O signals also routed to –ON_XX, -OE_XX, HS[5..0]
- VREF[2..0] used
- VBACKUP not used
- 11g, small-footprint PCB

PPM B1: C8051F120

- Utilizes SiLabs C8051F120-GQ (100-pin LQFP package)
- Regulates +5V_SYS & +5V_USB down to +3.3V for processor, VCC on MB and SD Card
- Uses on-chip POR
- Has local overcurrent protection / auto-reset
- Has optional high-speed crystal
- Has 1Mbit SRAM via P4.[7..5], P6.n, P7.n (multiplexed mode, paged)
- Has 6-pin FPC user debug header
- P0.n, P1.n, P2.n, P3.n, P4.0, AIN0.n, CP0/1 & DAC0/1 mapped to IO.[47..34, 30..0] on CSK bus
- I2C (P0.[7,6]) direct to SCL_SYS & SDA_SYS
- –ON_XX, -OE_XX, HS[5..0] on dedicated lines via P4 & P5
- VREF[2..0] used
- VBACKUP used for SRAM backup
- 17g, medium-footprint PCB

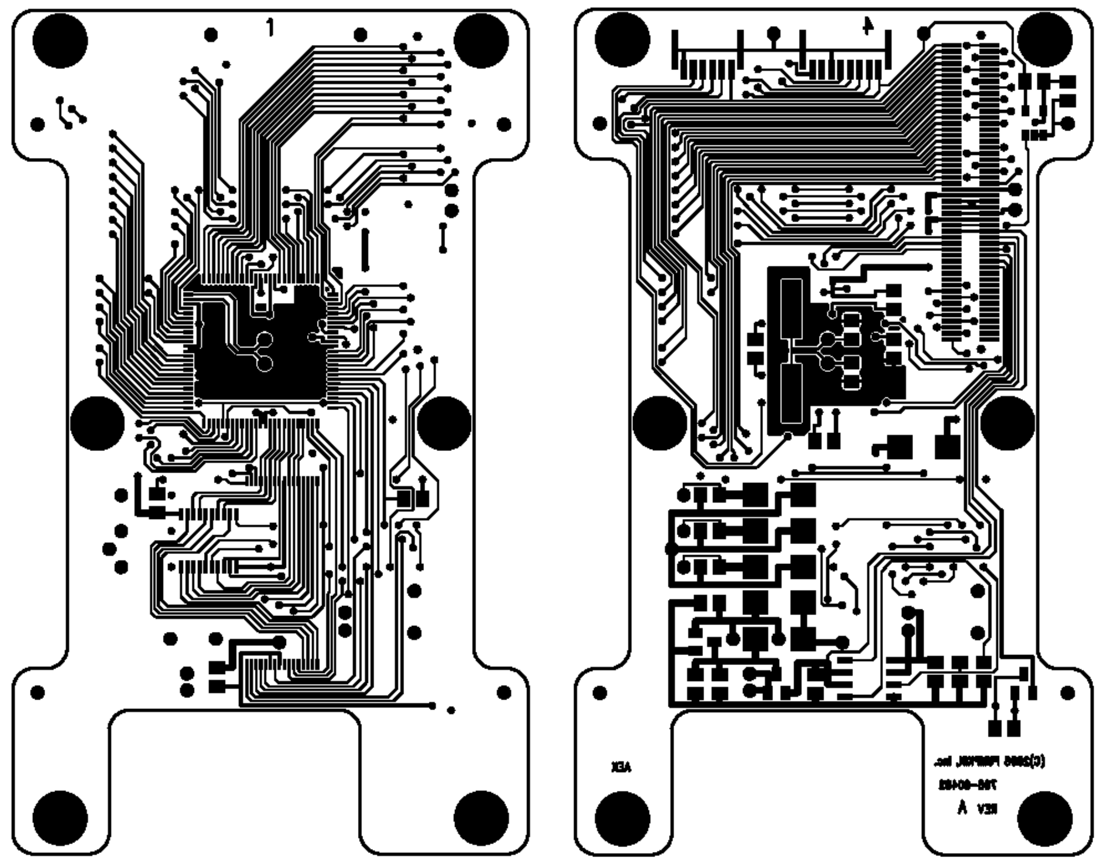
PPM A1 & B1



CubeSat Kit Pluggable Processor Modules PPM A1 (left) and PPM B1 (right)

PPM B1 PCB Design

- 4-layer PCB
- .007" traces / rules
- All SMT components
- 48.5 hrs design time
- Created with input from first customer



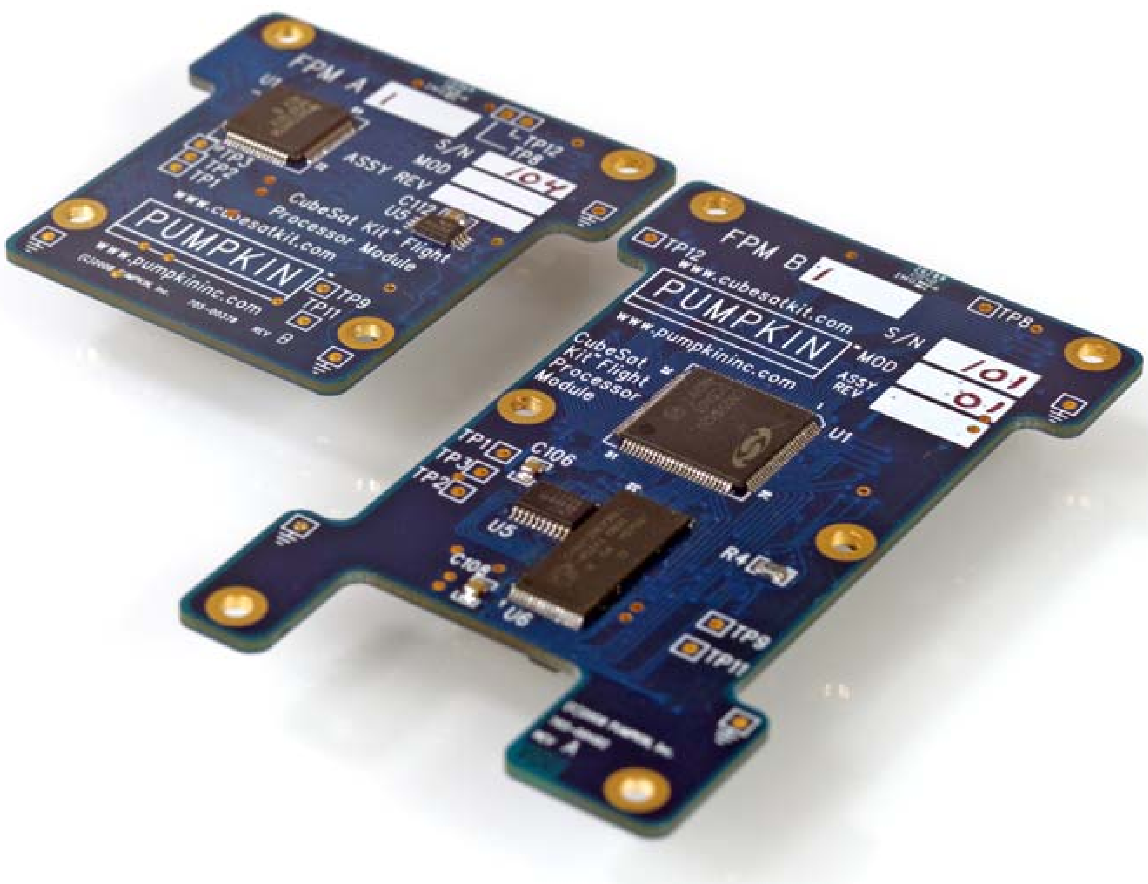
Artwork layers 1 & 4 of PPM B1 Rev A PCB

Review

- A PPM designer must resolve, specify and do:
  - Mechanical interface & packaging constraints
  - Electrical interface
    - I/O & bus signals
    - Programming / debug (e.g., JTAG)
    - Power & control signals
  - Schematics
  - PCB layout
  - Parts procurement
  - Assembly & test
  - Software drivers (e.g., SD card)

Conclusions

- CSK Hinge design fully vetted, now in production.
- Virtually ***any*** microprocessor / microcontroller / CPU can be used on a PPM, subject to volume & power constraints.
- Single-chip micros, processors with external memory, multi-processor systems, DSPs, CPU+SDR, CPU w/TMR Flash memory, etc. are all candidates for PPM integration. If it fits within the physical and power envelope of the open PPM specification, you ***can*** fly it!
- Existing software ***and*** hardware designs can be ported to the CubeSat Kit with the design of an appropriate PPM.
- Once compatible with the CubeSat Kit, your CubeSat Kit & PPM can utilize other COTS CSK-compatible hardware.



Q&A Session

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Appendix

- Speaker information
  - Dr. Kalman is Pumpkin's president and chief technology architect. He entered the embedded programming world in the mid-1980's. After co-founding Euphonix, Inc – the pioneering Silicon Valley high-tech pro-audio company – he founded Pumpkin, Inc. to explore the feasibility of applying high-level programming paradigms to severely memory-constrained embedded architectures. He is the creator of the Salvo RTOS and the CubeSat Kit. He holds two United States patents. He is a consulting professor in the Department of Aeronautics & Astronautics at Stanford University and directs the department's Space Systems Development Laboratory (SSDL). Contact Dr. Kalman at aek@pumpkininc.com.
- Acknowledgements

  - Pumpkin's Salvo and CubeSat Kit customers, whose real-world experience with our products helps us improve and innovate.

- CubeSat Kit information
  - More information on Pumpkin's CubeSat Kit can be found at http://www.cubesatkit.com/.
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