



How to Accommodate Additional Processors in the CubeSat Kit™

Andrew E. Kalman, Ph.D.

Slide 1





Introduction



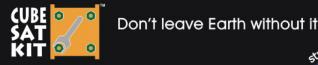
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Outline



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- Part III: Interfacing Additional Processors
- Part IV: Going it Alone
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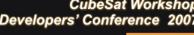
CubeSat Kit Architecture & **Processor**



- Versatile MCU-based architecture:
 - Modular approach w/ 90 x 96mm PCB form factor.
 - 104-pin stackable CSK Bus connectors form a backplane:
 - I/O, power, control, status, network, xcvr, switching, user-defined.
 - 48 I/O pins directly on CSK Bus.
 - +5V, +3.3V, V_{BATT} & V_{BACKUP} all on CSK Bus.
 - For uni- or multi-processor implementations.
- Every CSK module has full access to entire CSK Bus:
 - C&DH: source & endpoint for many signals.
 - EPS: deliver power to bus, status & control to C&DH.
 - COMM: handle Tx & Rx, use +3.3V for I/O, +5V for transmitter.
 - Payload: interface between C&DH and payload / experiment.













CubeSat Kit Module Stack Example









CubeSat Kit Bus Connectors

sense		H1 H-2X 1357911357913579135791357913579135791357	26-F 24 6 8 10 12 14 16 18 20 22 24 26 8 30 32 34 36 8 40 42 44 6 8 50 50 50 50 50 50 50 50 50 50 50 50 50	P5.6 P5.4 P5.2 P5.0 P4.6 P4.4 P4.2 P4.0 P3.6 P3.4 P3.2 P3.0 VREF+ VEREF+ VEREF+ VREF- +5V USB -RST MHX -RTS MHX -RTS MHX RXD MHX VBACKUP res. res. USER1 USER3 USER5	+5V_USB	agnd T	P6.7 P6.5 P6.3 P6.1 P1.7 P1.5 P1.3 P1.1 P2.7 P2.5 P2.3 P2.1 +5V VCC SYS GND AGND S0 S1 S2 S3 S4 S5 VBATT USER6 USER8 USER10	H2 H-2X 1 357911357192135722931335739143547951	26-F 24-68-10-11-11-11-11-11-11-11-11-11-11-11-11-	P6.6 P6.4 P6.2 P6.0 P1.6 P1.4 P1.2 P1.0 P2.6 P2.4 P2.2 P2.0 +5V VCC SYS GND GND GND S0 S1 S2 S3 S4 S5 VBATT USER7 USER9 USER11	+5V v	rcc_s	YS
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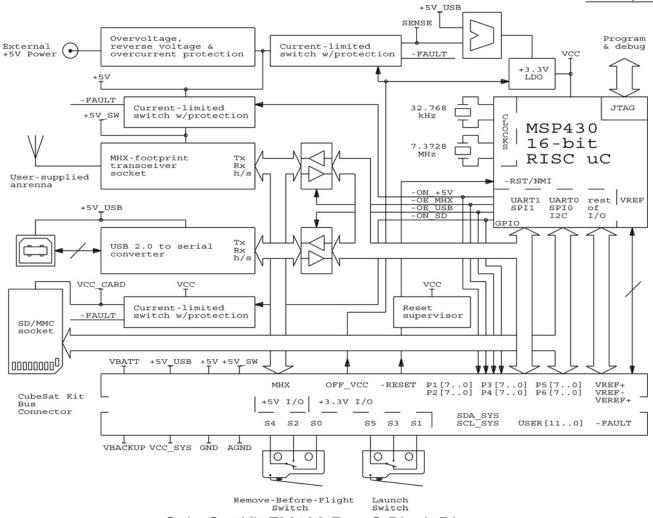
- CSK FM430 Flight Module features:
 - +5V supply, +3.3V core & I/O, reset via supervisor @ < +3.1V.
 - MSP430F1612 MCU w/5KB RAM & 55KB Flash, 48 +3.3V I/O (36 unallocated).
 - Extremely low-power operation (< 5mA run, < 40μA sleep).
 - 3 clocks: 32.768kHz, DCO (0-850kHz), 7.3728MHz.
 - Overcurrent, overvoltage, undervoltage & latch-up protection.
 - System-wide resources:
 - Flight MCU.

- SD card (mass storage) interface.
- Transceiver (MHX socket) / zero-power USB interface.
- Launch & Remove-Before-Flight switches.
- +5V external power jack, JTAG programming / debug interface.





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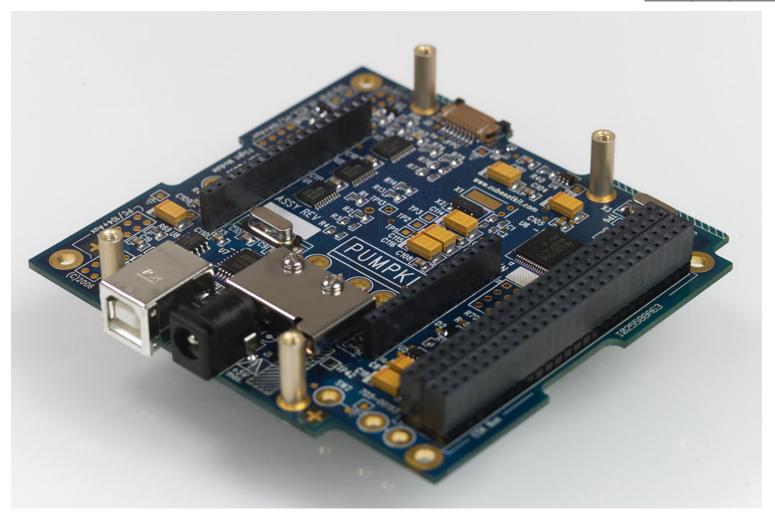


CubeSat Kit FM430 Rev C Block Diagram









CubeSat Kit FM430 Flight Module Rev C





Choosing Processors



- TI's 16-bit MSP430 RISC MCU
- Benefits:
 - Lowest-power MCU available, startup in 6μs.
 - Low-cost JTAG debugger & development boards.
 - Very C-friendly, good code density (esp. vs. 8-bit).
 - Versatile I/O, easy configuration, vectored interrupts.
 - Well supported, good tools & example code available.
 - Widely available (through distribution and as samples).
 - Good peripheral mix: USARTs (UART, SPI, I2C), DMA, ADC, DAC, WDT, counter/timers, etc.
- Limitations:
 - 64KB address space (MSP430X up to 1MB), no external memory.
 - Max clock 8MHz (new families 16 to 25MHz).
 - +3.6V max V_{CC}, < 2mA output drive, no +5V-tolerant I/O.
 - No PC host-like functions available (e.g. USB host, Ethernet).







Don't leave Earth without it



The FM430 Flight Module's MCU is well-suited to the C&DH role. With multitasking software it can handle:

- COM interface @ 19,200bps.
- SPI, I2C & async serial payload peripherals.
- FAT-based reading and writing to SD card mass memory.
- Control & monitoring of EPS & system power & health.
- Some PWM-based tasks (motor control, audio waveform output).
- More ...
- However, heavy computational loads involving e.g. noninteger divides / matrix inversions (e.g. for GPS waypoint calculations) or DSP-like signal processing exceed the MSP430's real-time capabilities.





Possible multiprocessor architectures in the CubeSat Kit:

- Multiple "lesser or equal" low-power MCUs (e.g. small PICs or AVRs or even MSP430s) offload end-node computing. E.g. network of I2C or SPI slaves with FM430's MSP430 Flight MCU as the master.
- "Coprocessor approach" where one or more powerful (and consequently power-hungry) processors are onboard to perform dedicated functions at low duty cycle (e.g. < 10%) under FM430's command. PC/104, other SBC, ARM7/ARM9, PowerPC, DSP, gumstix, etc. running Linux or Windows or other OS. In these designs the FM430's role may be secondary.
- Multiple FM430s in one CubeSat Kit (1.5U or larger) using wired or wireless connectivity between them.







Other reasons for adding additional processors:

- Already part of (sub-)payload hardware.
- Existing COTS software + hardware is ideally suited to a particular mission, or is only available solution.
- Processor testbeds (e.g. flight qualification of new processors).
- Sponsor- or partner-driven.

- Redundancy.
- Power requirements of additional processors will largely dictate how they are used, esp. in 1U CubeSats (1 - 5W total power). Most additional processors will spend their time asleep or powered off.
- Consider that from a mass and power standpoint, it's often more efficient to pack more functionality into a single processor than to spread it amongst multiple processors. K.I.S.S.



Interfacing Additional Processors



- CubeSat Kit module design is relatively straightforward:
 - Required:
 - Conform to CSK PCB module specification (footprint).
 - Power from +5V and/or +3.3V, reset properly (e.g. via supervisor).
 - All I/O to FM430 must be +3.3V, avoid overcurrent (> 2mA).
 - If used, limit +5V USB draw to available (< 500mA).</p>
 - FM430 Interface:
 - Standard I2C, SPI and async serial interfaces (all +3.3V I/O).
 - User-defined for unallocated I/O from/to FM430 or other devices.
 - Handshaking required to access FM430's local resources (e.g. SD card, USB).
 - Optional:
 - Drive +5V I/O to MHX transceiver, control +5V_SW.
 - Interface to —RESET, OFF VCC & -FAULT (o.c.), etc.
 - Use USER[11..0] bus in any way you want ... need not be +3.3V.







- FM430 hardware design for additional processors:
 - None FM430 architecture is already defined.
 - Any additional h/w (e.g. for RS422) must be implemented in the I/O space on another (i.e. user) module. Shared I/O must be pinned out properly on user modules!
- FM430 software design for additional processors:
 - Largely user-defined:
 - Native serial interfaces (I2C, SPI, simple async serial devices) are ready to go.
 - Non-native interfaces & protocols (e.g. RS422, CAN, SLIP) will require software protocol(s) to pass data among processors and share control of bus signals where necessary.



- A properly designed additional processor module will:
 - Conform to the CSK PCB module specification.
 - Fit inside a maximum volume of 90 x 96 x 15x(n+10)mm.
 - Run on +5V and/or +3.3V directly from the CSK Bus.
 - Connect to the minimum number of CSK Bus pins required to power the module and communicate with the FM430 and/or other processors at +3.3V.
 - Pass all unused CSK Bus pins on to other modules.
 - Be an enabling element of the responsive space approach that typifies CubeSats in particular and nanosatellites in general.



Going it Alone



- An alternative uni- or multiprocessor approach is to use module(s) other than the CubeSat Kit's FM430 Flight Module, i.e. use just the CubeSat Kit mechanicals (structure, etc.)
 - Drawbacks:
 - Available 90 x 96mm footprint limits choices (many PC/104 modules will not fit).
 - Design costs and times, lack of Pumpkin support, etc.
 - Useful FM430 features (extremely low power, USB, SD card) may not be present.
 - Inability to use other CSK modules (e.g. Clyde Space EPS).
 - Cannot draw support from CubeSat Kit community.
- 90 x 96mm PCB in the CubeSat Kit module / PC/104 footprint is mechanically compatible with the family of CubeSat Kit structures.



Examples



- Earlier CubeSat designs:
 - QuakeSat: 3U, with underclocked Linux PC/104 SBC
 - GeneSat-1: 3U, with PIC18-based C&DH & separate payload processor

■ MAST: separable 3U, with 3 identical PIC18-based TUI "Magic

Boards"

Current CubeSat Kit designs:

■ Libertad-1: 1U, with FM430

Delfi-C3: 3U, with FM430 & multiple I2C slaves

 BioLaunch-1: with FM430 & TMZ104 low-power SBC running Windows XP



CubeSat Kit Module Stack with TMZ104 above FM430





Summary



- The CubeSat Kit architecture can easily accommodate additional processors.
- A variety of multiprocessor architectures are possible.
- The rules for harmonious multiprocessor operation are relatively simply satisfied.





Q&A Session

Thank you for attending this Pumpkin seminar at the CubeSat Workshop Developers' Conference 2007!

Notice

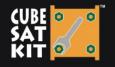


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Suggested Reading



- 1. MSP430x15x, MSP430x16x, MSP430x161x Mixed Signal Microcontroller, Texas Instruments Datasheet SLAS368D, October 2002.
- 2. MSP430x1xx Family User's Guide Revision F, Texas Instruments SLAU049F, 2006.
- 3. Salvo User Manual, Pumpkin, Inc., 2003.
- 4. CubeSat Kit FM430 Flight Module datasheet, Pumpkin, Inc., 2007.

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<u>Appendix</u>



Speaker information

Dr. Kalman is Pumpkin's president and chief technology architect. He entered the embedded programming world in the mid-1980's. After co-founding Euphonix, Inc – the pioneering Silicon Valley high-tech pro-audio company – he founded Pumpkin to explore the feasibility of applying high-level programming paradigms to severely memory-constrained embedded architectures. He holds two United States patents and is a consulting professor at Stanford University.

Acknowledgements

- Stanford Professors Bob Twiggs' and Jamie Cutler's continued support for the CubeSat Kit, and their inputs on enhancements and suggestions for future CubeSat Kit products, are greatly appreciated.
- Pumpkin's Salvo and CubeSat Kit customers, whose real-world experience with our products helps us improve and innovate.

Salvo, CubeSat Kit and CubeSat information

 More information on Pumpkin's Salvo RTOS and Pumpkin's CubeSat Kit can be found at http://www.pumpkininc.com/ and http://www.pumpkininc.com/ and http://www.cubesatkit.com/, respectively.

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