http://www.cubesatkit.com/

CubeSat Kit™ Development Board (DB)

Hardware Revision: E

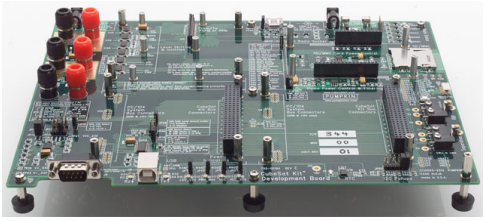
Single Board Computer Development Platform

Applications

- Laboratory platform for CubeSat Kit training, development, debugging & testing

Features

- Open architecture – accepts Pluggable Socketed Processor Modules (PSPMs) & Pluggable Processor Modules (PPMs)
- On-board +5V & +3.3V LDO regulators
- Code-compatible with CubeSat Kit Motherboard
- User-configurable RS-232 port / monitor
- Compatible with a wide range of supply and I/O voltages
- Extremely low (<10µA) quiescent current
- Integrated peripherals:
  - I2C real-time clock
  - 3V Lithium backup battery
  - USB 2.0 device interface for pre-launch communications, battery charging and power
  - MMC/SD card socket for mass storage (32MB to 2GB and beyond)
- Support for a wide range of transceivers
- Two stackable 104-pin CubeSat Kit Bus connectors includes processor's complete I/O space, user-assignable signals and more
- Extensible to multiprocessor architectures, with processor reset / NMI pin on bus
- Direct wiring for heavy-duty Remove-Before-Flight (battery) and Separation (power) switches
- Comprehensive overcurrent, overvoltage & undervoltage (reset) protection
- Independent latchup (device overcurrent) protection on critical subsystems
- Flexible dual-input-range high-power external DC power input
- Bus override for critical power and data/control paths
- Power consumption can be monitored externally
- Wiring-free module interconnect scheme
- PC/104-size footprint, with +5V and GND on PC/104 J1/J2 connectors



ORDERING INFORMATION

Pumpkin P/N 710-00297

Option Code	PPM Connector Height
/00 (standard)	+6mm

Contact factory for availability of optional configurations. Option code /00 shown.

CAUTION

Electrostatic Sensitive Devices

Handle with Care

- 6-layer gold-plated green-soldermask PCB with dual ground planes for enhanced signal integrity
- Compatible with Pumpkin's Salvo™ RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming
- Backwards-compatible with CubeSat Kit Rev. A through Rev. D Development Board

CHANGELOG

Rev.	Date	Author	Comments
A	20120327	AEK	Initial version. Based on Development Board Rev D datasheet.
B	20120417	AEK	Corrected **VREF1** & **VREF2** pin numbers on **H1**.

OPERATIONAL DESCRIPTION

The CubeSat Kit Development Board (DB) is the fifth generation of Pumpkin's line of single-board computers (SBCs) designed for use in the CubeSat Kit and elsewhere. The DB is intended as a laboratory-grade platform for CubeSat Kit training, development, debugging and testing. Its components are arranged so as to provide maximum simultaneous access to all of the subsystems of the CubeSat Kit core architecture that are present on the DB. It is not intended – and indeed, it cannot be made to fit within – any CubeSat. Instead, CubeSats are developed using the DB, and then the proven and tested CubeSat modules and the DB software is migrated to the CubeSat Motherboard (MB) during integration.

The DB includes all of the core features of the MB, with the following additional features:

- A second CubeSat Kit Bus connector to support a second stack of modules
- A second external DC power in, with local +5V and +3.3V regulators[1]
- A user-configurable RS232 port with DB9 connector
- A variety of jumpers for configuration and circuit isolation
- The ability to accept socketed processors

The MB is an electrically *identical* subset of the DB. When outfitted with the same PPM, [2] they are completely code compatible – i.e. CubeSat Kit firmware developed on the DB will run on the MB without rebuilding, and vice versa.

The DB has a socket to accommodate PPMs. PPMs can be sourced from Pumpkin, third parties or can be created by CubeSat Kit end-users. Thus, a wide range of potential processors (e.g. MSP430, 8051, AVR®, PICmicro®, ARM®, x86, FPGA, ASIC, etc.) can be used with the DB via a suitable PPM.

The DB has a flexible power scheme that permits the use of PPMs with different power and I/O requirements. All of the DB's on-board peripheral I/O (RTC, MHX interface, USB & SD Card) is level-shifted and zero-power-isolated to interface with PPMs at any I/O voltage from +1.65V to +5.5V.

The DB provides the PPM socket with all of the CubeSat Kit Bus Connector I/O and power signals, as well as some dedicated and special-purpose DB signals.[3]

[1] Essentially, a simple desktop Electrical Power Systems (EPS).

[2] Herein PPM will refer to a PPM, a Pluggable Socketed Processor Module (PSPM) or a PPM adapter. The latter two are only suitable for use on DBs, and not on MBs.

[3] The only signals from the CubeSat Kit Bus Connector that are not presented at the PPM connector are the **S0**-**S5** signals (Remove-Before-Flight and Separation Switches) and direct MHX interface signals (e.g., **-RTS_MHX**, etc.).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature [4]	T_A	-40 to +85	ºC
Voltage on **+5V_USB** bus		-0.3 to +6	V
Voltage on **+5V_SYS** bus			
Voltage on **PWR_MHX** bus			
Voltage on **VCC_SYS** bus			
Voltage on **–FAULT** open-collector output			
Voltage on local **VCC** bus		-0.3 to +5.5	V
Voltage on any I/O pin		-0.3 to (**VCC** + 0.3)	V
Voltage on local **VCC_SD** bus		-0.3 to +3.6	V
Voltage on **VBACKUP** bus		-0.3 to +3.6	V
Voltage at external +5V power connector **J1** [5]		-25 to +25	V
DC current through any pin of PPM Connector	I_{PIN1_MAX}	1.2	A
DC current through any pin of CubeSat Kit Bus Connector [6]	I_{PIN2_MAX}	3	A
DC current through external +5V power connector **J1** [7]	I_{EXT_MAX}	4	A
DC current through Remove-Before-Flight or Separation Switches [8]	I_{SW_MAX}	10	A

[4] Does not include any SD card fitted to the DB. Typical commercial SD card operating temperatures are 0ºC to + 55ºC. Typical industrial extended temperature range SD cards operate over -40ºC to + 85ºC.

[5] Voltages between 0V and +5.5V are passed through to **+5V_SYS** on the CubeSat Kit Bus.

[6] Current derating is a function of temperature, number of pins in use and connector geometry. Users should consult the connector manufacturer's test results for more information. See *Connectors*, below, for manufacturer and part number information as used on the MB.

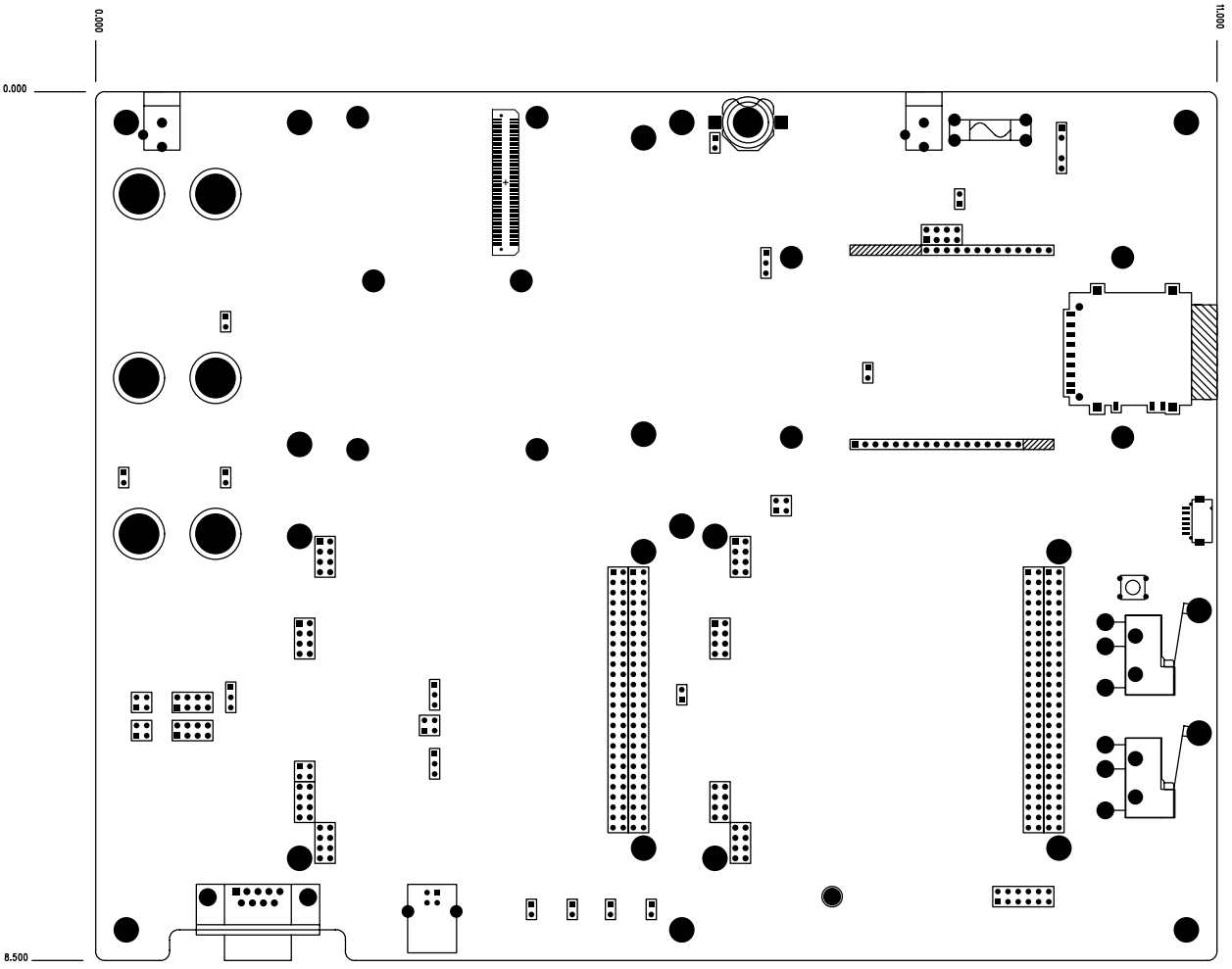
[7] Limited by a fast-blo 4A 5x20mm user-replaceable fuse fuse.

[8] Make only. Not rated for repetitive make and break cycles of dc current. AC rating for switches alone. The RBF Switche **SW1** and the Separation Switch **SW2** are typically wired by the user directly to the DB to simplify S[5..0] bus connections. User should analyze temperature rise on inner layers as a function of currents passed through RBF and Separation Switches. For high-current applications, wiring directly to the switch (instead of indirectly through the CubeSat Kit Bus connector's S[5..0] pins and the DB PCB) may be preferred. Switches are Cherry P/N E62-10H and E62-10K.

PHYSICAL CHARACTERISTICS

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
PCB width	US letter size (8.5" x 11")			279		mm
PCB length				216		mm
PCB thickness				1.6		mm
Mating external power jack dimensions	Outer diameter				5.5	mm
	Internal diameter		2.1			
CubeSat Kit Bus Connector terminal pitch	Horizontal or vertical distance to nearest terminal			2.54		mm
Switch terminal hole diameter	For C, NO & NC switch terminals [9]			2.54		mm
Compatible coin cell battery dimensions	Diameter			12		mm
	Height		2.0	2.5	2.5	mm

SIMPLIFIED MECHANICAL LAYOUT [10]



[9] Common, Normally Open and Normally Closed.
[10] Dimensions in inches.

ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Operating Voltage	I/O voltage for all on-board peripherals except RTC and SD Card interface	V_{CC}	1.65		5.5	V
	RTC [11]		2.7		5.5	V
	SD Card interface [12]	V_{CC_SD}		3.3		V
Maximum external dc voltage	External dc voltage increased until protection circuitry forces disconnect	V_{EXT_TRIP}			5.5	V
Backup battery voltage	Feeds **VBACKUP** through **R20** (4.7kΩ).	V_{BT1}		3.0	3.5	V
Voltage drop from external dc power connector to **+5V_SYS** [13]	I_{IN} = 5mA	V_{EXT_DROP}			10	mV
	I_{IN} = 4A			400		
Operating current	Typical operation	I_{OP}		500		µA
	All control outputs inactive, PPM asleep	I_{SLEEP}		5	10	µA
RTC crystal frequency	No external capacitors	f_{CLK_RTC}	32.768 ± 0.001			kHz
USB bus current [14]	Powered over USB	I_{USB_MAX}			500	mA
Overcurrent trip point for SD Card socket	Set by **R61**	I_{TRIP_SD}		170		mA
Overcurrent trip point for MHX transceiver socket	Set by **R23**	I_{TRIP_MHX}		2400		mA
Time to switch between **+5V_SYS** and **+5V_USB** power sources	Automatic				1	µs
Data rate through any on-board isolator (**U1**-**U3**, **U16**-**U18**)	May be reduced (due to parasitic capacitance) by inline resistors (e.g., **R9**-**R12**, **R59**) where fitted with non-zero values		50			MHz

USB DEVICE CHARACTERISTICS

Parameter	Conditions / Notes	Value
Speed [15]	USB 2.0 compatible	Low Speed (1.5Mbps) Full Speed (12Mbps)
Vendor ID (VID)		0403
Product ID (PID)		F020
Reported options	Unique serial number	/07F0
Reported serial number	Format: PUdddddd	unique to each unit
Required driver	See CubeSat Kit website	provided by Pumpkin

[11] DB is fitted with M41T81S RTC. **Vcc** of +2.7V or higher is required for proper operation. Operation at lower values of **Vcc** requires the removal of the RTC and/or its substitution with one capable of running at voltages lower than +2.7V.

[12] SD Card standard requires operation at +3.3V. Lower-voltage SD cards can be accommodated by PPM supplying **VCC_SD** with an appropriate voltage, and by using SD cards specified for lower operating voltages.

[13] Measured at +5V system test point **TP9**. External +5V passes through a fuse and an active overvoltage protection circuit before reaching system +5V. DB PCB is implemented with 2oz copper to minimize resistance of power traces.

[14] The DB's USB interface is configured at the factory to report a maximum current of 500mA for a bus-powered device to any attached USB host.

[15] Actual throughput is dependent on coding in and configuration of processor, and is often much lower.

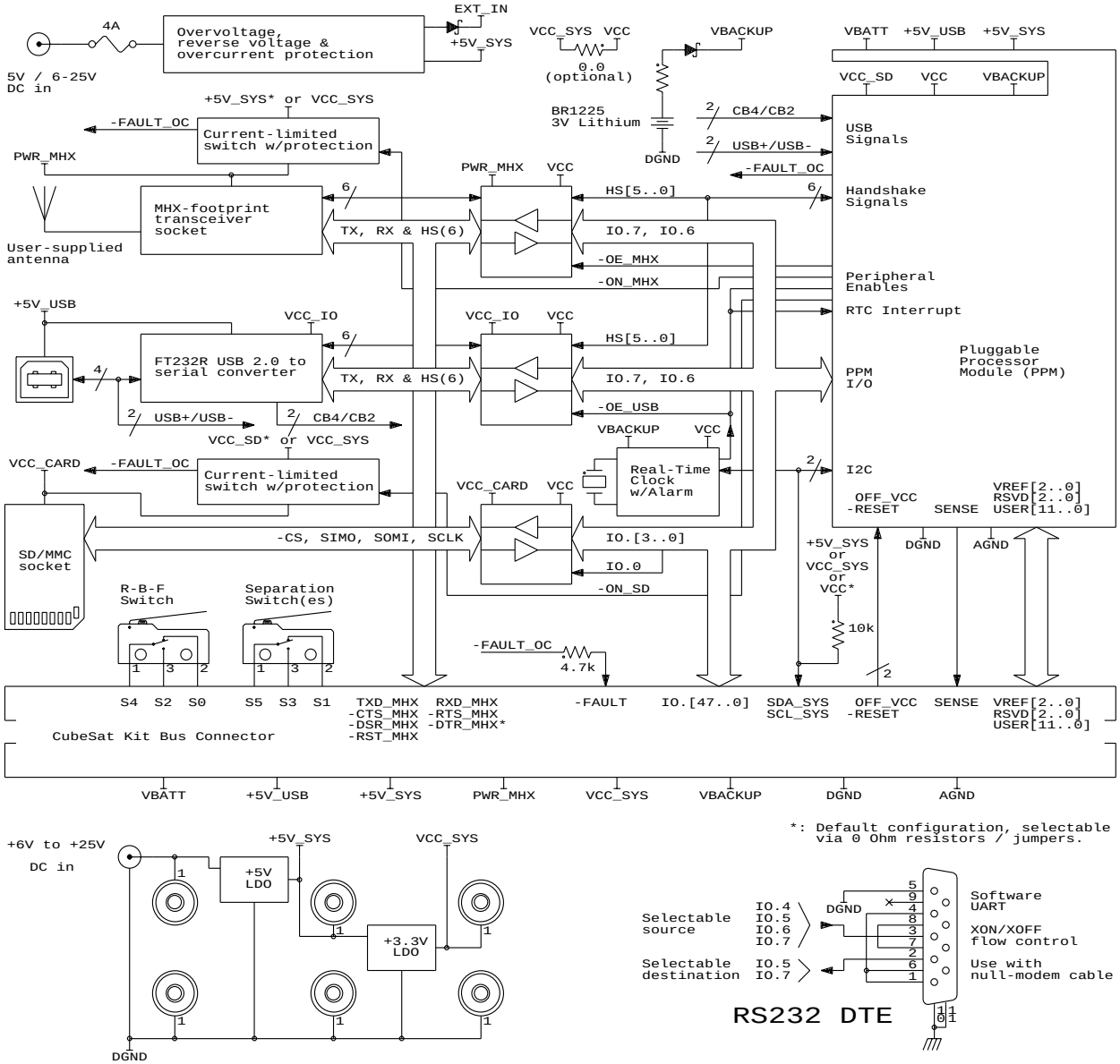
Backup Battery

The DB has a replaceable BR1225 3V Lithium coin cell to serve as a backup battery for real-time clocks and other components requiring battery backup of volatile information.

Battery BT1 is held in place by a coin cell battery holder in one corner of the underside of the DB. The all-metal battery holder is oriented in such a way that once installed onto a CubeSat Kit Base Plate, the battery cannot slide out of its battery holder and is thereby physically restrained along five of six axes. However, since the battery has a conductive outer shell, excessive movement of the battery along its insertion / removal axis could result in a short if it were to contact the Base Plate. Therefore insulating Kapton tape and/or an epoxy or silicone adhesive should be applied to the battery and battery holder.

Alternately, the customer can feed **VBACKUP** on the CubeSat Kit bus via their own backup battery located elsewhere in the system.

BLOCK DIAGRAM



PPM PIN DESCRIPTIONS

The PPM connector **H10** connects resources on the DB and accessible via the CubeSat Kit Bus connector to a PPM.[16]

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.[17] Signals marked with an '*' are associated with dedicated peripherals on the DB. They may also be used with off-board peripherals through the proper use of DB peripheral enables and DB power control.

The *potential* for a pin's function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

Inputs are signals *from* the DB *to* the PPM's processor **U1** or other circuitry. *Outputs* are signals *from* the PPM's processor **U1** or other circuitry *to* the DB.

H10
LSS-150-02-L-DV

<->	IO.23	1	2	IO.47	<->
<->	IO.22	3	4	IO.46	<->
<->	IO.21	5	6	IO.45	<->
<->	IO.20	7	8	IO.44	<->
<->	IO.19	9	10	IO.43	<->
<->	IO.18	11	12	IO.42	<->
<->	IO.17	13	14	IO.41	<->
<->	IO.16	15	16	IO.40	<->
<->	IO.15	17	18	IO.39	<->
<->	IO.14	19	20	IO.38	<->
<->	IO.13	21	22	IO.37	<->
<->	IO.12	23	24	IO.36	<->
<->	IO.11	25	26	IO.35	<->
<->	IO.10	27	28	IO.34	<->
<->	IO.9	29	30	IO.33	<->
<->	IO.8	31	32	IO.32	<->
-->	IO.7 *	33	34	IO.31	<->
<--	IO.6 *	35	36	IO.30	<->
-->	IO.5	37	38	IO.29	<->
<--	IO.4	39	40	IO.28	<->
<--	IO.3 *	41	42	IO.27	<->
-->	IO.2 *	43	44	IO.26	<->
<--	IO.1 *	45	46	IO.25	<->
<--	IO.0 *	47	48	IO.24	<->
	+5V_USB	49	50	+5V_USB	
	+5V_SYS	51	52	+5V_SYS	
	VCC_SD	53	54	VCC_SD	
	VCC	55	56	VCC	
	DGND	57	58	DGND	
	AGND	59	60	AGND	
	VBATT	61	62	VBATT	
	VBACKUP	63	64	VBACKUP	
	VREF0	65	66	-FAULT_OC	-->
	VREF1	67	68	SENSE	-->
	VREF2	69	70	-RESET	<--
	RSVD0	71	72	OFF_VCC	<--
	RSVD1	73	74	SDA_SYS	<->
	RSVD2	75	76	SCL_SYS	-->
-->	USBDP/CB4	77	78	USER0	
-->	USBDM/CB2	79	80	USER1	
<--	-ON_SD	81	82	USER2	
<--	-ON_MHX	83	84	USER3	
<--	-OE_MHX	85	86	USER4	
<->	-OE_USB/-INT	87	88	USER5	
-->	HS0	89	90	USER6	
-->	HS1	91	92	USER7	
-->	HS2	93	94	USER8	
<--	HS3	95	96	USER9	
<--	HS4	97	98	USER10	
<--	HS5	99	100	USER11	

[16] Not included. PPMs are purchased separately from MBs.
[17] The CubeSat Kit's system peripherals are numbered from 0 onwards (e.g., UART0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal.

PPM PIN DESCRIPTIONS – I/O

Name	Pin	I/O	CSKB	Description
IO.0	H10.47	I/O	•	**-CS_SD**. Controls SD Card interface. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.1	H10.45	I/O	•	**SDO0**. SPI master data out. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.2	H10.43	I/O	•	**SDI0**. SPI master data in. *Part of the DB's SD card interface. Normally configured as an input to the PPM processor.*
IO.3	H10.41	I/O	•	**SCK0**. SPI clock. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.4	H10.39	I/O	•	**UTX0**. Tx0 data out. *Often configured as an output from the PPM processor.*
IO.5	H10.37	I/O	•	**URX0**. Rx0 data in. *Often configured as an input to the PPM processor.*
IO.6	H10.35	I/O	•	**UTX1**. Tx1 data out to MHX transceiver or USB. *Part of the DB's MHX/USB interface. Normally configured as an output from the PPM processor.*
IO.7	H10.33	I/O	•	**URX1**. Rx1 data in from MHX transceiver or USB. *Part of the DB's MHX/USB interface. Normally configured as an input to the PPM processor.*
IO.8	H10.31	I/O	•	General-purpose I/O.
IO.9	H10.29	I/O	•	General-purpose I/O.
IO.10	H10.27	I/O	•	General-purpose I/O.
IO.11	H10.25	I/O	•	General-purpose I/O.
IO.12	H10.23	I/O	•	General-purpose I/O.
IO.13	H10.21	I/O	•	General-purpose I/O.
IO.14	H10.19	I/O	•	General-purpose I/O.
IO.15	H10.17	I/O	•	General-purpose I/O.
IO.16	H10.15	I/O	•	General-purpose I/O.
IO.17	H10.13	I/O	•	General-purpose I/O.
IO.18	H10.11	I/O	•	General-purpose I/O.
IO.19	H10.9	I/O	•	General-purpose I/O.
IO.20	H10.7	I/O	•	General-purpose I/O.
IO.21	H10.5	I/O	•	General-purpose I/O.
IO.22	H10.3	I/O	•	General-purpose I/O.
IO.23	H10.1	I/O	•	General-purpose I/O.
IO.24	H10.48	I/O	•	General-purpose I/O.
IO.25	H10.46	I/O	•	General-purpose I/O.
IO.26	H10.44	I/O	•	General-purpose I/O.
IO.27	H10.42	I/O	•	General-purpose I/O.
IO.28	H10.40	I/O	•	General-purpose I/O.
IO.29	H10.38	I/O	•	General-purpose I/O.
IO.30	H10.36	I/O	•	General-purpose I/O.
IO.31	H10.34	I/O	•	General-purpose I/O.
IO.32	H10.32	I/O	•	General-purpose I/O.
IO.33	H10.30	I/O	•	General-purpose I/O.
IO.34	H10.28	I/O	•	General-purpose I/O.
IO.35	H10.26	I/O	•	General-purpose I/O.
IO.36	H10.24	I/O	•	General-purpose I/O.
IO.37	H10.22	I/O	•	General-purpose I/O.
IO.38	H10.20	I/O	•	General-purpose I/O.
IO.39	H10.18	I/O	•	General-purpose I/O.
IO.40	H10.16	I/O	•	General-purpose I/O. *Normally configured as analog input **AN0** to the PPM processor.*

IO.41	H10.14	I/O	•	General-purpose I/O. *Normally configured as analog input **AN1** to the PPM processor.*
IO.42	H10.12	I/O	•	General-purpose I/O. *Normally configured as analog input **AN2** to the PPM processor.*
IO.43	H10.10	I/O	•	General-purpose I/O. *Normally configured as analog input **AN3** to the PPM processor.*
IO.44	H10.8	I/O	•	General-purpose I/O. *Normally configured as analog input **AN4** to the PPM processor.*
IO.45	H10.6	I/O	•	General-purpose I/O. *Normally configured as analog input **AN5** to the PPM processor.*
IO.46	H10.4	I/O	•	General-purpose I/O. *Normally configured as analog input **AN6** to the PPM processor.*
IO.47	H10.2	I/O	•	General-purpose I/O. *Normally configured as analog input **AN7** to the PPM processor.*

PPM PIN DESCRIPTIONS – Power

Name	Pin	I/O	CSKB	Description
+5V_USB	H10.49 H10.50	–	•	+5V USB power. From USB host. Powers on-board USB-to-serial converter and PPM.
+5V_SYS	H10.51 H10.52	–	•	+5V system power. From EPS or external +5V connector. Powers some on-board peripherals and PPM.
VCC_SD	H10.53 H10.54	–		SD Card power. Nominally +3.3V. Sourced from PPM or from **VCC_SYS** via **R58**.
VCC	H10.55 H10.56	–		DB power and I/O level. From +1.65V to +5.5V. Sourced from PPM or from **VCC_SYS** via **R68**.
DGND	H10.57 H10.58	–	•	Digital ground.
AGND	H10.59 H10.60	–	•	Analog ground.
VBATT	H10.61 H10.62	–	•	Battery voltage. EPS-dependent. Typically +7V to +10V.
VBACKUP	H10.63 H10.64	–	•	Battery backup voltage (e.g. for RTC). From DB's 3V Lithium battery **BT1**.

PPM PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	CSKB	Description
VREF0	H10.65	-	•	Intended for analog voltage references.
VREF1	H10.67	-	•	Intended for analog voltage references.
VREF2	H10.69	-	•	Intended for analog voltage references.

PPM PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	CSKB	Description
RSVD0	H10.71	–	•	Not connected. Reserved for future use.
RSVD1	H10.73	–	•	Not connected. Reserved for future use.
RSVD2	H10.75	–	•	Not connected. Reserved for future use.

PPM PIN DESCRIPTIONS – DB-Specific

Name	Pin	I/O	CSKB	Description
CB4	H10.77	I		Configurable CBUS4 signal from FT232R USB chip **U7**.
USBDP				When **U7** is not fitted and **R56** is fitted, provides the '+' half of the USB differential signal pair from **J3** to the PPM processor.

CB2	H10.79	I		Configurable CBUS2 signal from FT232R USB chip **U7**.
USBDM				When **U7** is not fitted and **R57** is fitted, provides the '-' half of the USB differential signal pair from **J3** to the PPM processor.
-ON_SD	H10.81	O		Control signal for SD Card power. Active LOW, pulled high on DB. When active, enables **VCC_CARD** on DB, thereby powering SC Card socket and SD Card level translators / isolators **U17** & **U18**. *Normally configured as a digital output from the PPM processor.*
-ON_MHX	H10.83	O		Control signal for MHX socket power. Active LOW, pulled high on DB. When active, enables **PWR_MHX** on DB, thereby powering MHX socket and MHX level translators / isolators **U2** & **U3**. *Normally configured as a digital output from the PPM processor.*
-OE_MHX	H10.85	O		Control signal for MHX interface. Active LOW, pulled high on DB. When active, enables signals to pass through MHX level translators / isolators **U2** & **U3**. *Normally configured as a digital output from the PPM processor.*
-OE_USB	H10.87	O		Control signal for USB interface. Active LOW, pulled high on DB. When active, enables signals to pass through USB level translators / isolators **U1** & **U16**. *Normally configured as a digital output from the PPM processor.*
-INT		I		Output from RTC's –IRQ open-collector output. When properly configured, can be used to interrupt Processor via RTC. *Normally configured as a digital input to the PPM processor.*
HS0	H10.89	I		Handshake signal. –RTS (USB) or –CTS (MHX). *Normally an input to the PPM processor. Requires that **R10** be fitted on the DB.*
HS1	H10.91	I		Handshake signal. –DTR (USB) or –DSR (MHX). *Normally an input to the PPM processor. Requires that **R11** be fitted on the DB.*
HS2	H10.93	I		Handshake signal. –PWE (USB) or –DCD (MHX). *Normally an input to the PPM processor. Requires that **R12** be fitted on the DB.*
HS3	H10.95	O		Handshake signal. –CTS (USB) or –RTS (MHX). *Normally an output from the PPM processor. Requires that **R75** be fitted on the DB.*
HS4	H10.97	O		Handshake signal. –RI (USB) or –DTR (MHX). *Normally an output from the PPM processor. Requires that **R76** be fitted on the DB.*
HS5	H10.99	O		Handshake (reset) signal. –RST (USB) or –RST (MHX). *Normally an output from the PPM processor. Requires that **R77** be fitted on the DB.*

PPM PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	CSKB	Description
-FAULT_OC	H10.66	O		Open-collector output from PPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to –FAULT_OC on DB.
SENSE	H10.68	O	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PPM implementation.
-RESET	H10.70	I	•	Reset signal to PPM's reset supervisor. Active LOW.
OFF_VCC	H10.72	I	•	Control signal to PPM's power circuit(s). Active HIGH.

PPM PIN DESCRIPTIONS – I2C Bus

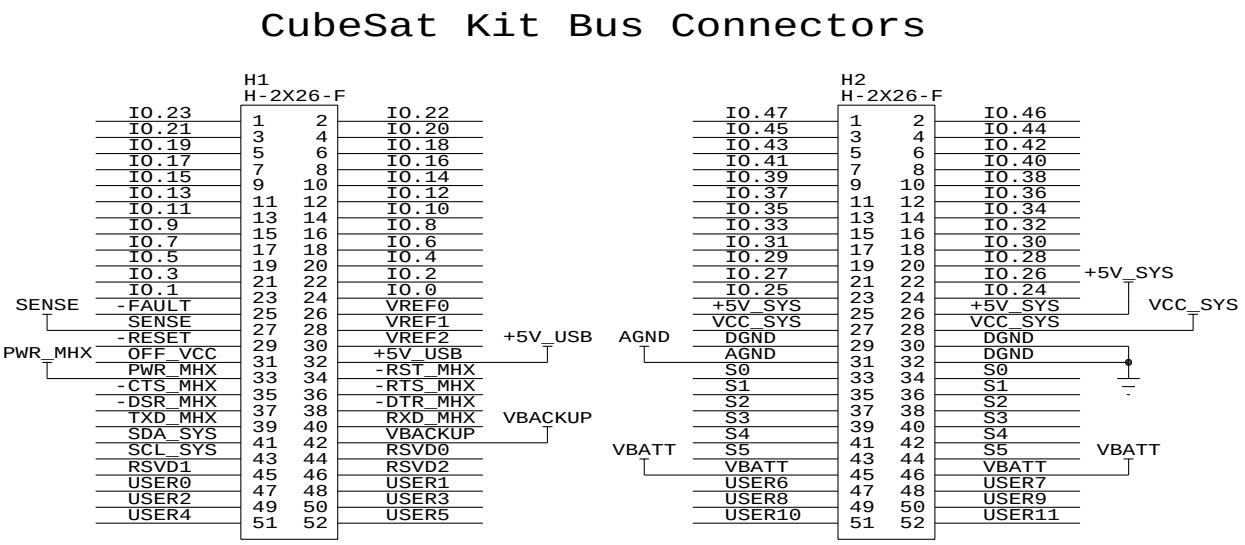
Name	Pin	I/O	CSKB	Description
SDA_SYS	H10.74	I/O	•	I2C data. *Normally configured as an I2C data input/output to/from the processor.*
SCL_SYS	H10.76	O	•	I2C clock. *Normally configured as an I2C clock output from the PPM processor.*

PPM PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	CSKB	Description
USER0	H10.78	I/O	•	User-defined.
USER1	H10.80	I/O	•	User-defined.
USER2	H10.82	I/O	•	User-defined.
USER3	H10.84	I/O	•	User-defined.
USER4	H10.86	I/O	•	User-defined.
USER5	H10.88	I/O	•	User-defined.
USER6	H10.90	I/O	•	User-defined.
USER7	H10.92	I/O	•	User-defined.
USER8	H10.94	I/O	•	User-defined.
USER9	H10.96	I/O	•	User-defined.
USER10	H10.98	I/O	•	User-defined.
USER11	H10.100	I/O	•	User-defined.

CubeSat Kit Bus PIN DESCRIPTIONS [18]

Those signals that are connected directly between the CubeSat Kit Bus connectors and the PPM connector are tagged under the PPM label below.



CubeSat Kit Bus PIN DESCRIPTIONS – I/O

Name	Pin	I/O	PPM	Description
IO.0	H1.24	I/O	•	**-CS_SD**. Controls SD Card interface. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.1	H1.23	I/O	•	**SDO0**. SPI master data out. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.2	H1.22	I/O	•	**SDI0**. SPI master data in. *Part of the DB's SD card interface. Normally configured as an input to the PPM processor.*
IO.3	H1.21	I/O	•	**SCK0**. SPI clock. *Part of the DB's SD card interface. Normally configured as an output from the PPM processor.*
IO.4	H1.20	I/O	•	**UTX0**. Tx0 data out. *Often configured as an output from the PPM processor.*
IO.5	H1.19	I/O	•	**URX0**. Rx0 data in. *Often configured as an input to the PPM processor.*
IO.6	H1.18	I/O	•	**UTX1**. Tx1 data out to MHX transceiver or USB. *Part of the DB's MHX/USB interface. Normally configured as an output from the PPM processor.*
IO.7	H1.17	I/O	•	**URX1**. Rx1 data in from MHX transceiver or USB. *Part of the DB's MHX/USB interface. Normally configured as an input to the PPM processor.*
IO.8	H1.16	I/O	•	General-purpose I/O.
IO.9	H1.15	I/O	•	General-purpose I/O.
IO.10	H1.14	I/O	•	General-purpose I/O.
IO.11	H1.13	I/O	•	General-purpose I/O.
IO.12	H1.12	I/O	•	General-purpose I/O.
IO.13	H1.11	I/O	•	General-purpose I/O.
IO.14	H1.10	I/O	•	General-purpose I/O.
IO.15	H1.9	I/O	•	General-purpose I/O.
IO.16	H1.8	I/O	•	General-purpose I/O.

[18] The fact that the CubeSat Kit Bus has 104 pins (like PC/104) is purely coincidental – the original CubeSat Kit Bus used in the Rev A and Rev B FM430 had only 80 pins, and was expanded in Rev C to 104 pins.

IO.17	H1.7	I/O	•	General-purpose I/O.
IO.18	H1.6	I/O	•	General-purpose I/O.
IO.19	H1.5	I/O	•	General-purpose I/O.
IO.20	H1.4	I/O	•	General-purpose I/O.
IO.21	H1.3	I/O	•	General-purpose I/O.
IO.22	H1.2	I/O	•	General-purpose I/O.
IO.23	H1.1	I/O	•	General-purpose I/O.
IO.24	H2.24	I/O	•	General-purpose I/O.
IO.25	H2.23	I/O	•	General-purpose I/O.
IO.26	H2.22	I/O	•	General-purpose I/O.
IO.27	H2.21	I/O	•	General-purpose I/O.
IO.28	H2.20	I/O	•	General-purpose I/O.
IO.29	H2.19	I/O	•	General-purpose I/O.
IO.30	H2.18	I/O	•	General-purpose I/O.
IO.31	H2.17	I/O	•	General-purpose I/O.
IO.32	H2.16	I/O	•	General-purpose I/O.
IO.33	H2.15	I/O	•	General-purpose I/O.
IO.34	H2.14	I/O	•	General-purpose I/O.
IO.35	H2.13	I/O	•	General-purpose I/O.
IO.36	H2.12	I/O	•	General-purpose I/O.
IO.37	H2.11	I/O	•	General-purpose I/O.
IO.38	H2.10	I/O	•	General-purpose I/O.
IO.39	H2.9	I/O	•	General-purpose I/O.
IO.40	H2.8	I/O	•	General-purpose I/O. *Normally configured as analog input **AN0** to the PPM processor.*
IO.41	H2.7	I/O	•	General-purpose I/O. *Normally configured as analog input **AN1** to the PPM processor.*
IO.42	H2.6	I/O	•	General-purpose I/O. *Normally configured as analog input **AN2** to the PPM processor.*
IO.43	H2.5	I/O	•	General-purpose I/O. *Normally configured as analog input **AN3** to the PPM processor.*
IO.44	H2.4	I/O	•	General-purpose I/O. *Normally configured as analog input **AN4** to the PPM processor.*
IO.45	H2.3	I/O	•	General-purpose I/O. *Normally configured as analog input **AN5** to the PPM processor.*
IO.46	H2.2	I/O	•	General-purpose I/O. *Normally configured as analog input **AN6** to the PPM processor.*
IO.47	H2.1	I/O	•	General-purpose I/O. *Normally configured as analog input **AN7** to the PPM processor.*

CubeSat Kit Bus PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	PPM	Description
VREF0	H1.26	-	•	Intended for analog voltage references.
VREF1	H1.28	-	•	Intended for analog voltage references.
VREF2	H1.30	-	•	Intended for analog voltage references.

CubeSat Kit Bus PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	PPM	Description
RSVD0	H1.44	–	•	Not connected. Reserved for future use.
RSVD1	H1.45	–	•	Not connected. Reserved for future use.
RSVD2	H1.46	–	•	Not connected. Reserved for future use.

CubeSat Kit Bus PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	PPM	Description
SDA_SYS	H1.41	I/O	•	I2C data. *Normally configured as an I2C data input/output to/from the processor.*
SCL_SYS	H1.43	O	•	I2C clock. *Normally configured as an I2C clock output from the PPM processor.*

CubeSat Kit Bus PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	PPM	Description
-FAULT	H1.25	O	•	Open-collector output. Active LOW. Active when an overcurrent fault condition is detected by any of the DB's or PPM's latchup prevention overcurrent switches. With series 4.7kΩ resistor. Normally pulled up externally to **VCC_SYS** or **+5V_SYS**.
SENSE	H1.27	O	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PPM implementation.
-RESET	H1.29	I	•	Reset signal to PPM's reset supervisor. Active LOW.
OFF_VCC	H1.31	I	•	Control signal to PPM's power circuit(s). Active HIGH.

CubeSat Kit Bus PIN DESCRIPTIONS – RBF and Separation Switches

Name	Pin	I/O	PPM	Description
S0	H2.33 H2.34	–		Switch terminal. Normally connected to RBF Switch normally closed (NC) terminal.
S1	H2.35 H2.36	–		Switch terminal. Normally connected to Separation Switch normally closed (NC) terminal.
S2	H2.37 H2.38	–		Switch terminal. Normally connected to RBF Switch normally open (NO) terminal.
S3	H2.39 H2.40	–		Switch terminal. Normally connected to Separation Switch normally open (NO) terminal.
S4	H2.41 H2.42	–		Switch terminal. Normally connected to RBF Switch common (C) terminal.
S5	H2.43 H2.44	–		Switch terminal. Normally connected to Separation Switch common (C) terminal.

CubeSat Kit Bus PIN DESCRIPTIONS – Power

Name	Pin	I/O	PPM	Description
VBATT	H2.45 H2.46	–	•	Battery voltage. EPS-dependent. Typically +7V to +10V.
+5V_USB	H1.32	–	•	+5V USB power. From USB host.
+5V_SYS	H2.25 H2.26	–	•	+5V system power. From EPS or external +5V connector.
PWR_MHX	H1.33	–	•	MHX transceiver power. Derived from **+5V_SYS** or **VCC_SYS** system power. Under PPM control. The current used by the MHX transceiver is (**+5V_SYS** – **PWR_MHX**) / 75mΩ or (**VCC_SYS** – **PWR_MHX**) / 75mΩ, depending on the source of MHX power. Can be overridden by feeding **+5V_SYS** or **VCC_SYS** directly into **PWR_MHX**.
VBACKUP	H1.42	–	•	Battery backup voltage (e.g. for RTC). From DB's 3V Lithium battery **BT1**.
VCC_SYS	H2.27 H2.28	–	•	VCC system power. Normally generated by EPS. Not normally connected to DB's local **VCC**.
AGND	H2.31	–	•	Analog ground.

DGND	H2.29 H2.30 H2.32	–	•	Digital ground.

CubeSat Kit Bus PIN DESCRIPTIONS – Transceiver Interface

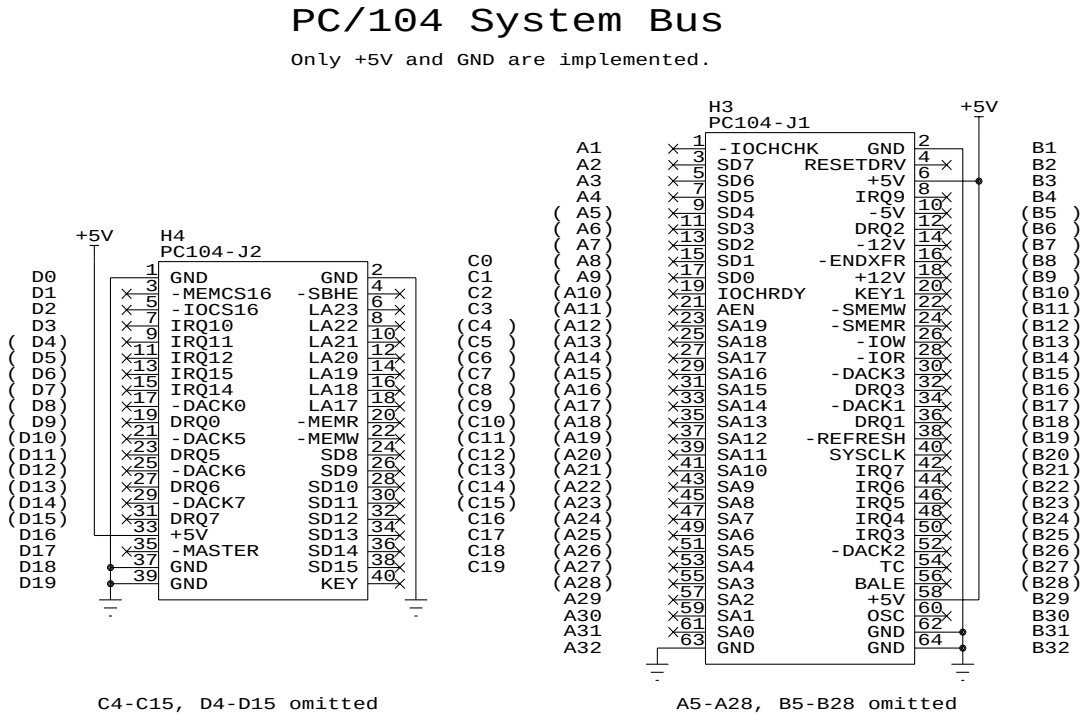
Name	Pin	I/O	PPM	Description
-RST_MHX	H1.34	I		Reset input to transceiver. Active LOW.
-CTS_MHX	H1.35	O		Clear-to-send output from transceiver. Active LOW.
-RTS_MHX	H1.36	I		Request-To-Send input to transceiver. Active LOW.
-DSR_MHX	H1.37	O		Data Set Ready output from transceiver. Active LOW.
-DXX_MHX	H1.38	I		**-DTR_MHX** when **JP25** is jumpered 1-2:[19] Data Transmit Ready input to transceiver. Active LOW. **-DCD_MHX** when **JP25** is jumpered 2-3: Data Carrier Detect output from transceiver. Active LOW.
TXD_MHX	H1.39	I		Transmit data input to transceiver. Idles HIGH.
RXD_MHX	H1.40	O		Receive data output from transceiver. Idles HIGH.

CubeSat Kit Bus PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	PPM	Description
USER0	H1.47	I/O	•	User-defined.
USER1	H1.48	I/O	•	User-defined.
USER2	H1.49	I/O	•	User-defined.
USER3	H1.50	I/O	•	User-defined.
USER4	H1.51	I/O	•	User-defined.
USER5	H1.52	I/O	•	User-defined.
USER6	H2.47	I/O	•	User-defined.
USER7	H2.48	I/O	•	User-defined.
USER8	H2.49	I/O	•	User-defined.
USER9	H2.50	I/O	•	User-defined.
USER10	H2.51	I/O	•	User-defined.
USER11	H2.52	I/O	•	User-defined.

[19] Default.

PC/104 System Bus PIN DESCRIPTIONS



The DB implements a subset of the PC/104 specification in the form of two connectors that provide only +5V and GND for PC/104 modules. Only a total of 32 pins are implemented, 16 on **H3** and 16 on **H4**. By adding up to four 8-pin connectors to the DB, PC/104 modules can be plugged directly into the DB to obtain +5V power and GND. No other connections between the PC/104 bus and the CubeSat Kit Bus are provided.

CONNECTORS

Item	Description	Source	Part Number	Application
1	52-pin non-stackthrough	Samtec[20]	ESQ-126-37-G-D	CubeSat Kit Bus connector for non-stackthrough applications (e.g., DB option /00).
2	52-pin stackthrough	Samtec	ESQ-126-39-G-D	CubeSat Kit Bus connector for stackthrough applications (e.g., DB option /10).
3	52-pin	Samtec	SSQ-126-22-G-D	CubeSat Kit Bus connector 10mm extension.
4	8-pin non-stackthrough	Samtec	ESQ-104-37-G-D	CubeSat Kit PC/104 power connector for non-stackthrough applications.
5	8-pin stackthrough	Samtec	ESQ-104-39-G-D	CubeSat Kit PC/104 power connector for stackthrough applications.
6	8-pin	Samtec	SSQ-104-22-G-D	CubeSat Kit PC/104 power connector 10mm extension.
7	100-pin, hermaphroditic	Samtec	LSS-150-02-L-DV	PPM connector (standard, +6mm)

Items 1-6: Non-stackthrough connectors are normally fitted only to an DB and form an endpoint to the CubeSat Kit Bus connector stack. Stackthrough connectors are normally fitted to all other modules (e.g. EPS modules). The normal stacking height is 15mm between modules. The 10mm extension can be used to increase this distance, e.g. to 25mm. 8-pin connectors are used to provide +5V and GND (only) to PC/104 modules. A 15mm extension can be accomplished via a stackthrough connector.

[20] http://www.samtec.com/, 1-800-SAMTEC9.

This connector information is provided for reference only.

REPLACEMENT FUSES

The overcurrent fuse **F1** protects only against overcurrent conditions drawing too much current from the external +5V dc supply. It is soldered in place. The replacement fuse is LittleFuse 0451004.MRL, 4A, 125V, fast-acting Nano SMF Fuse, and is available e.g. through Digi-Key®. Should replacement be required, it should be replaced by the factory or by a qualified electronics technician.

BACKWARDS COMPATIBILITY

DB Rev E is fully backwards-compatible with DB Rev D.

MHX WIRELESS TRANSCEIVER COMPATIBILITY

The MB is designed to interface directly to Microhard Corporation's[21] line of MHX OEM wireless transceiver modules, and any other footprint-compatible transceivers. The mechanical interface is through four M2.5 F/F threaded standoffs at a prescribed height of 15.5mm above the MB PCB. The electrical interface is through the MB's **H5** connectors, which connect the MHX module to the MB via the MHX pins 1-17 and 21-33 only.[22] Because of minor physical differences between the earlier (e.g., MHX-2400) and later (e.g., MHX-2420) Microhard transceivers, the MB as supplied from the factory supports only later transceivers. The MB uses a high-side switch for **PWR_MHX** capable of supplying currents to the transceiver in excess of the 1.2A. Either **+5V_SYS** or **VCC_SYS** can be the source of **MHX_PWR**, based on the fitment of **JP24**.

MULTIPLE / REDUNDANT SEPARATION SWITCHES

The Rev E DB PCB can support a second, independent Separation Switch **SW4** by mounting it directly above **SW2**. When a second Separation Switch is used, the end-user must facilitate connecting its terminals to those of the primary Separation Switch (**SW2**), if used in such a manner.

EXTERNAL DC POWER INPUT

The DB accepts external DC power and implements overvoltage, reverse voltage and overcurrent protection at DC power jack **J1**. **J1** can be used in two distinct and different ways: for 5Vdc power in, or for 6-25Vdc power in. When the voltage at **J1** is under +5.5Vdc, power is passed to **+5V_SYS** and to connector **J19**. For voltages above +5.5Vdc, an active circuit isolates **J1** from **+5V_SYS** and power is passed only to connector **J19**. In all cases, up to 4A can pass through **J1**. *A conforming 5.5mm/2.1mm plug must be used at all times to ensure the proper operation of the MB's overvoltage protection circuitry on **J1**.*

For implementations with an architectural power dependency on +5V_SYS, an external +5Vdc power supply can provide up to 20W of power to the DB via **J1**. For implementations dependent on a different bus power voltage, **J1**'s dual-input-range feature can be used. For example, in an architecture with a four-cell Li-Ion battery chemistry,[23] 14.8V can be applied at **J1** and can be routed to an endpoint within the system via a user harness from the DB connector **J19**.[24] In this configuration, the DB can source up to 100W through **J1**. See the DB schematics for more information.[25]

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[21] http://www.microhardcorp.com/.

[22] These pins were originally No Connect (NC) on the MHX-2400 and similar modules. Later versions use these pins. The functionality of most of these additional pins is not required to operate these newer MHX modules (e.g,. MHX-2420), and hence they are backwards-compatible with the earlier MHX modules.

[23] Li-Ion nominal cell voltage is 3.7V, peak is typically 4.2V. The nominal battery voltage for four cells in series – a 4S1P configuration – is therefore 14.8V.

[24] A 1x5 0.100" pitch square-pin male header with the center pin removed.

[25] A high-power Schottky diode **D15** is present in-line between **J1** and **J19**. Sophisticated users wishing to implement advanced functions – e.g. using **J1** as a means to charge batteries within a CubeSat – may choose to bypass **D15** so as to be able to sense battery voltage. Contact the factory for more details.

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