

CubeSat Kit[™] Pluggable Processor Module (PPM) D1 Hardware Revision: A

PPM with Microchip® PIC24 for CubeSat Kit Motherboard

Applications

- CubeSat nanosatellite control, C&DH, TT&C
- · General-purpose low-power computing for CubeSat Kit architecture
- Remote sensing for harsh environments

Features

- For CubeSat Kit Motherboard (MB)
- Microchip® PIC24FJ256GA110 16-bit microcontroller (MCU)
- 256KB program memory, 16KB on-chip SRAM
- Up to 16MIPS @ 32MHz
- Integrated peripherals:
 - 4 UARTs, 3 SPIs, 3 I2Cs
 - 16-channel 10-bit 500ksps ADC
 - 5 16-bit timers
 - 9 capture inputs
 - 9 compare / PWM outputs
 - 3 analog comparators
 - RTCC, CTMU, WDT, ICD, JTAG, etc.
- Majority of Peripheral Pin Selects mapped to PPM connector
- 8.000MHz & 32.768kHz clock crystals
- AT25DF641 64Mbit SPI serial Flash memory
- Independent latchup (device overcurrent) protection
- Independent external reset supervisor (POR/BOR)
- Medium-size PPM footprint
- 4-layer gold-plated blue-soldermask PCB
- Compatible with Pumpkin's Salvo[™] RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming



Prototype shown.

ORDERING INFORMATION

Pumpkin P/N 710-00527

Option Code	PPM Connector Height
/00 (standard)	+3mm

Contact factory for availability of optional configurations. Option code /00 shown

CAUTION



Electrostatic Sensitive Devices



Handle with Care



CHANGELOG

Rev.	Date	Author	Comments
A	20090713	AEK	Initial revision.
В	20090728	AEK	Updated PPM pin descriptions and image, minor nomenclature changes, max heights of PCB, brought nomenclature inline with PPM A1/A2/A3, added additional signal information, other minor changes.
С	20090728	AEK	Fixed some incorrect PIC24 signal names, resolved minor formatting inconsistencies.
D	20090808	AEK	Added photo.
E	20091021	AEK	Added typical operating current.

OPERATIONAL DESCRIPTION

PPM D1 enables CubeSat Kit customers to utilize the PIC24 processor on a CubeSat Kit Motherboard (MB). PPM D1 uses the 100-pin PIC24FJ256GA110-I/PF, with a wide selection of on-chip peripherals. Additionally, a 64Mbit external serial Flash memory is present for off-chip storage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature	T _A	-40 to +85	°C
Voltage on +5v_USB bus			
Voltage on +5v_svs bus		-0.3 to +6.0	V
Voltage on -FAULT_OC open-collector output			
Voltage on vcc bus		-0.3 to +3.6	V
Voltage on vcc_sp bus		-0.3 10 +3.0	v
Voltage on any mixed analog/digital processor I/O pin		-0.3 to	
		(VCC + 0.3)	V
Voltage on any digital-only processor I/O pin		-0.3 to 6.0	
DC current through any pin of PPM connector H1	I_{PIN_MAX}	1.2	A

Refer to the PIC24FJxxxGAx10 family datasheet for additional absolute maximum ratings associated with processor **U1**, especially per-pin current limits.

PHYSICAL CHARACTERISTICS

Parameter	Conditions / Notes	Symbol	Min	Тур	Max	Units
Mass				17		g
Height of components above PCB					2	mm
Height of components below PCB ¹					4	mm
PCB width				54.6		mm
PCB length	Medium-size PPM			89.5		mm
PCB thickness				1.6		mm

SIMPLIFIED MECHANICAL LAYOUT ²

PPM D1 is implemented on a medium-size PPM PCB, as shown below.



¹ Not including connector H1.

² Dimensions in inches.

ELECTRICAL CHARACTERISTICS

(T = 25°C, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes	Symbol	Min	Тур	Max	Units
Reset voltage	+5v_svs reduced until MCU resets	V _{RESET_MAX}			3.1	V
Operating Voltage		V _{CC}		3.3		V
SD Card Voltage		V _{CC_SD}		3.3		V
	Typical operation ³	I _{OP}		20		mA
Operating current	All control outputs inactive, PPM asleep	I _{SLEEP}		TBD	TBD	μA
Primary crystal frequency		f_{CLK_OSC}	8	3.00 ± 0.0	1	MHz
Secondary crystal frequency		fclk_sosc	32	.768 ± 0.0	01	kHz
Overcurrent trip point for vcc	Set by R3	I _{TRIP_VCC}		220		mA
Time to switch between +5v_sys and +5v_usb power sources	Automatic				1	μs

³ Running CubeSat Kit test\test1 application v1.2.2.

BLOCK DIAGRAM

PPM D1 provides regulated and current-limited +3.3V power, an external POR/BOR reset supervisor, JTAG and ICD interfaces for programming and debugging, two clock sources, an external high-speed 64Mbit serial Flash memory, connections to all 48 I/O pins of the PPM connector, dedicated MB control and radio handshaking signals, a single-point analog/digital ground, and a careful assignment of the mappable and non-mappable PIC24 peripherals to the PPM connector and CubeSat Kit bus. A few of the PIC24's 100 pins are not used.



PPM PIN DESCRIPTIONS

The PPM connector **H1** connects the PPM to resources residing on the MB and to resources accessible via the CubeSat Kit Bus connector.⁴

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.⁵ Signals marked with an ^{**} are associated with dedicated peripherals on the MB. They may also be used with off-board peripherals through the proper use of MB peripheral enables and MB power control.

The *potential* for a pin's function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

Inputs are signals *from* the MB *to* the PPM's processor **U1** or other circuitry. *Outputs* are signals *from* the PPM's processor **U1** or other circuitry *to* the MB.



⁴ Not included. MBs are purchased separately from PPMs.

⁵ The CubeSat Kit's system peripherals are numbered from 0 onwards (e.g., UART0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal. The PIC24's peripheral nomenclature begins with 1 (e.g., U1, SPI1, etc.), and is used when referring to peripherals, signals and registers internal to the PIC24.

PPM PIN DESCRIPTIONS - I/O

Name	Pin	I/O	CSKB	Description
				-CS_SD. Controls SD Card interface. From RE5 (U1.3). Part
IO.0	H1.48	I/O	•	of the MB's SD card interface. RE5 is normally configured as
				a simple output.
				SDO0. SPI0 (master) data out. From RP15 (U1.53). Part of
10.1	H1.46	I/O	•	the MB's SD card interface. RP15 is normally configured as
				output function SDO1.
				SDI0. SPI0 (master) data in. To RPI44 (U1.54). Part of the
10.2	H1.44	I/O	•	MB's SD card interface. RPI44 is normally configured as
				input function SDI1.
				SCK0. SPI0 clock. From RP4 (U1.69). Part of the MB's SD
IO.3	H1.42	I/O	•	card interface. RP4 is normally configured as output function
				SCK10UT.
IO.4	H1.40	I/O	•	UTX0. Tx0 data out. From RP16 (U1.51). RP16 is normally
10.4	111.40	1/0	•	configured as output function U1TX.
IO.5	H1.38	I/O	•	URX0. Rx0 data in. To RP30 (U1.52). RP30 is normally
10.5	111.50	1/0	•	configured as input function U1RX.
				UTX1. Tx1 data out. From RP17 (U1.50). Part of the MB's
IO.6	H1.36	I/O	•	MHX/USB interface. RP17 is normally configured as output
				function U2TX.
				URX1. Rx1 data in. To RP10 (U1.49). Part of the MB's
IO.7	H1.34	I/O	•	MHX/USB interface. RP10 is normally configured as input
				function U2RX.
				-SS1. SPI1 slave select. From RP27 (U1.14). Part of the
IO.8	H1.32	I/O	•	second SPI interface. RP27 is normally configured as output
				function SS2OUT. Can also be used as general-purpose I/O.
				SDO1. SPI1 (master) data out. From RP19 (U1.12). Part of
10.9	H1.30	I/O	•	the second SPI interface. RP19 is normally configured as
		".		output function SDO2. Can also be used as general-purpose
				Ι/Ο.
				SDI1. SPI1 (master) data in. To RP26 (U1.11). Part of the
10.10	H1.28	I/O	•	second SPI interface. RP26 is normally configured as input
				function SDI2. Can also be used as general-purpose I/O.
				SCK1. SPI1 clock. From RP21 (U1.10). Part of the second
10.11	H1.26	I/O	•	SPI interface. RP21 is normally configured as output function
				SCK2OUT. Can also be used as general-purpose I/O.
				-URTSO. UARTO request-to-send. From RP5 (U1.48). Part of
10.12	H1.24	I/O	•	the first UART interface. RP5 is normally configured as output
				function -U1RTS. Can also be used as general-purpose I/O.
TO 12	114.00			-UCTSO. UARTO clear-to-send. To RPI43 (U1.47). Part of the
10.13	H1.22	I/O	•	first UART interface. RPI43 is normally configured as input
				function –U1CTS. Can also be used as general-purpose I/O.
				-URTS1. UART1 request-to-send. From RP31 (U1.39). Part
10.14	H1.20	I/O	•	of the second UART interface. RP31 is normally configured
				as output function –U2RTS. Can also be used as general-purpose I/O.
				-UCTS1. UART1 clear-to-send. To RPI31 (U1.40). Part of the
				second UART interface. RPI31 is normally configured as
10.15	H1.18	I/O	•	input function –U2CTS. Can also be used as
				general-purpose I/O.
IO.16	H1.16	I/O	•	General-purpose I/O. To/from RP2 (U1.68).
10.17	H1.14	1/0	•	General-purpose I/O. To/from RP22 (U1.78).
10.18	H1.12	1/0	•	General-purpose I/O. To/from RP122 (01.70).
10.10	H1.10	1/0	•	General-purpose I/O. To/from RP142 (01.73).
10.13	111.10	"0	-	$\sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{i$

	-			
TO 00	114.0			SCL1. I2C1 clock. From SCL2 (U1.58). Part of the second I2C
10.20	H1.8	I/O	•	interface. SCL2 is normally configured as an I2C clock output.
		_		Can also be used as general-purpose I/O.
TO 01	111.6		•	SDA1. I2C1 data. To/from SDA2 (U1.59). Part of the second
10.21	H1.6	I/O	•	I2C interface. SDA2 is normally configured as an I2C data
		_		input/output. Can also be used as general-purpose I/O.
TO 00				SCL2. I2C2 clock. To/from SCL3 (U1.4). Part of the third I2C
10.22	H1.4	I/O	•	interface. SCL3 is normally configured as an I2C clock output.
		-		Can also be used as general-purpose I/O.
TO 00	114.0			SDA2. I2C2 data. To/from SDA3 (U1.5). Part of the third I2C
10.23	H1.2	I/O	•	interface. SDA3 is normally configured as an I2C data
70.04		1/0		input/output. Can also be used as general-purpose I/O.
10.24	H1.47	I/O	•	General-purpose I/O. To/from RF1 (U1.88).
10.25	H1.45	I/O	•	General-purpose I/O. To/from RF0 (U1.87).
IO.26	H1.43	I/O	•	General-purpose I/O. To/from RG1 (U1.89).
IO.27	H1.41	I/O	•	General-purpose I/O. To/from RG0 (U1.90).
				SCL1*. I2C1 clock (alternate). To/from ASCL2 (U1.66).
10.28	H1.39	I/O	•	Provides an alternate location for the second I2C interface. If
10110	111.00	".		used, ASCL2 is normally configured as an I2C clock output.
				Can also be used as general-purpose I/O.
				SDA1*. I2C1 data (alternate). To/from ASDA2 (U1.67).
10.29	H1.37	I/O	•	Provides an alternate location for the second I2C interface. If
	111.07	"		used, ASCL3 is normally configured as an I2C data
				input/output. Can also be used as general-purpose I/O.
				INT1. External interrupt. To RPI33 (U1.18). RPI33 is
IO.30	H1.35	I/O	•	normally configured as input function INT1. Can also be used
				as general-purpose I/O.
				INT2. External interrupt. To RPI34 (U1.19). RPI34 is
10.31	H1.33	I/O	•	normally configured as input function INT2. Can also be used
				as general-purpose I/O.
IO.32	H1.31	I/O	•	AN8 . Analog input 8. To AN5 (U1.20). Can also be used as
				general-purpose I/O.
IO.33	H1.29	I/O	•	AN9 . Analog input 9. To AN4 (U1.21). Can also be used as
		-		general-purpose I/O.
IO.34	H1.27	I/O	•	AN10 . Analog input 10. To AN3 (U1.22). Can also be used as
		_		general-purpose I/O.
IO.35	H1.25	I/O	•	AN11 . Analog input 11. To AN2 (U1.23). Can also be used as
				general-purpose I/O.
IO.36	H1.23	I/O	•	an12 . Analog input 12. To an1 (U1.24). Also used for PGEC
				(ICD clock). Can also be used as general-purpose I/O.
IO.37	H1.21	I/O	•	AN13 . Analog input 13. To AN0 (U1.25). Also used for PGED
				(ICD data). Can also be used as general-purpose I/O.
IO.38	H1.19	I/O	•	AN14 . Analog input 14. To AN6 (U1.26). Can also be used as
				general-purpose I/O.
IO.39	H1.17	I/O	•	AN15 . Analog input 15. To AN7 (U1.27). Can also be used as
				general-purpose I/O.
IO.40	H1.15	I/O	•	ANO . Analog input 0. To AN8 (U1.32). Can also be used as
		+		general-purpose I/O.
IO.41	H1.13	I/O	•	AN1 . Analog input 1. To AN9 (U1.33). Can also be used as general-purpose I/O.
		+ +		AN2 . Analog input 2. To AN10 (U1.34). Can also be used as
IO.42	H1.11	I/O	•	
		+ +		general-purpose I/O.
IO.43	H1.9	I/O	•	AN3 . Analog input 3. To AN11 (U1.35). Can also be used as
		+ +		general-purpose I/O. AN4. Analog input 4. To AN12 (U1.41). Can also be used as
IO.44	H1.7	I/O	•	general-purpose I/O.
				general-pulpose I/O.

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10.45	H1.5	I/O	•	AN5 . Analog input 5. To AN13 (U1 .42). Can also be used as general-purpose I/O.
10.46	H1.3	I/O	•	AN6 . Analog input 6. To AN14 (U1.43). Can also be used as general-purpose I/O.
IO.47	H1.1	I/O	٠	AN7 . Analog input 7. To AN15 (U1.44). Can also be used as general-purpose I/O.

PPM PIN DESCRIPTIONS – Power

Name	Pin	I/O	CSKB	Description
+5V_USB	H1.49 H1.50	-	•	+5V USB power. From USB host. Powers PPM.
+5V_SYS	H1.51 H1.52	-	•	+5V system power. From EPS or external +5V connector. Powers PPM.
VCC_SD	H1.53 H1.54	-		+3.3V SD Card power. From PPM's vcc.
vcc	H1.55 H1.56	-		+3.3V PPM power, MB power and I/O level. From PPM LDO U4 using +5v_sys and/or +5v_USB.
DGND	H1.57 H1.58	_	•	Digital ground.
AGND	H1.59 H1.60	-	•	Analog ground.
VBATT	H1.61 H1.62	-	•	Not connected.
VBACKUP	H1.63 H1.64	-	•	Not connected.

PPM PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	CSKB	Description
VREF0	H1.66	-	•	Positive analog voltage reference. To/from VREF+ (U1.29).
VREF1	H1.68	-	•	Not connected.
VREF2	H1.70	-	•	Negative analog voltage reference. To/from VREF- (U1.28).

PPM PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	CSKB	Description
RSVD0	H1.72	_	•	Not connected. Reserved for future use.
RSVD1	H1.74	_	•	Not connected. Reserved for future use.
RSVD2	H1.76	_	•	Not connected. Reserved for future use.

PPM PIN DESCRIPTIONS – MB-Specific

Name	Pin	I/O	CSKB	Description
CB4	H1.78	1		Not connected.
USBDP	111.70	1		Not connected.
CB2	114 00			Not composited
USBDM	H1.80	I		Not connected.
-ON_SD	H1.82	0		Control signal for SD Card power. From RE4 (U1.100). Active LOW, pulled high on the MB. When active, enables VCC_CARD on the MB, thereby powering SC Card socket and SD Card level translators / isolators. <i>Normally configured as a digital output</i> .
-ON_MHX	H1.84	0		Control signal for MHX socket power. From RE3 (U1.99). Active LOW, pulled high on the MB. When active, enables PWR_MHX on the MB, thereby powering MHX socket and MHX level translators / isolators. <i>Normally configured as a</i> <i>digital output</i> .

-OE_MHX	H1.86	0	Control signal for MHX interface. From RE2 (U1 .98). Active LOW, pulled high on the MB. When active, enables signals to pass through MHX level translators / isolators. <i>Normally configured as a digital output.</i>
-OE_USB	- H1.88	0	Control signal for USB interface. From RC1 (U1.6). Active LOW, pulled high on the MB. When active, enables signals to pass through USB level translators / isolators. <i>Normally configured as a digital output.</i>
-INT		I	Output from RTC's -IRQ open-collector output. To RPI38 (U1.6). When properly configured, can be used to interrupt Processor via MB RTC. <i>Normally configured as a digital input</i> <i>with change-on input interrupt capability.</i>
нзо	H1.90	I	Handshake signalRTS (USB) or -CTS (MHX). To RPI41 (U1.9). Can be configured as an external interrupt to U1 or input handshake signal via its Peripheral Pin Select. Requires that R10 be fitted on the MB.
HS1	H1.92	I	Handshake signalDTR (USB) or -DSR (MHX). To RPI40 (U1.8). Can be configured as an external interrupt to U1 or input handshake signal via its Peripheral Pin Select. Requires that R11 be fitted on the MB.
HS2	H1.94	I	Handshake signalPWE (USB) or -DCD (MHX). To RPI39 (U1.7). Can be configured as an external interrupt to U1 or input handshake signal via its Peripheral Pin Select. Requires that R12 be fitted on the MB.
нз 3	H1.96	0	Handshake signalCTS (USB) or -RTS (MHX). From RP20/RD5 (U1.82). Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that R75 be fitted on the MB.
HS4	H1.98	0	Handshake signalRI (USB) or -DTR (MHX). From RP23/RD2 (U1.77). Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that R76 be fitted on the MB.
HS 5	H1.100	0	Handshake (reset) signalRST (USB) or -RST (MHX). From RP24/RD1 (U1.76). Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that R77 be fitted on the MB.

PPM PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	CSKB	Description
-FAULT_OC	H1.65	0		Open-collector output from PPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to -FAULT_OC on the MB.
SENSE	H1.67	-	•	Can be used to measure PPM's current consumption. The current used by the PPM from a single source is (source – $sense$) / 75m Ω . Depends on PPM implementation.
-RESET	H1.69	I	Reset signal to PPM's reset supervisor. Active LOW.	
OFF_VCC	H1.71		Control signal to PPM's power circuit(s). Active HIGH.	

PPM PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	CSKB	B Description	
SDA SYS	H1.73	I/O	•	I2C data. To/from SDA1 (U1.56). Part of the first I2C interface. SDA1 is normally configured as an I2C data	
	111.70	"0		input/output. Can also be used as general-purpose I/O.	
SCL_SYS	H1.75	0	•	I2C clock. From SCL1 (U1.57). Part of the first I2C interface. SCL1 is normally configured as an I2C clock output. Can also be used as general-purpose I/O.	

Name	Pin	I/O	CSKB	Description	
USER0	H1.77	I/O	•	Not connected.	
USER1	H1.79	I/O	•	Not connected.	
USER2	H1.81	I/O	•	Not connected.	
USER3	H1.83	I/O	•	Not connected.	
USER4	H1.85	I/O	•	Not connected.	
USER5	H1.87	I/O	•	Not connected.	
USER6	H1.89	I/O	•	Not connected.	
USER7	H1.91	I/O	•	Not connected.	
USER8	H1.93	I/O	•	Not connected.	
USER9	H1.95	I/O	•	Not connected.	
USER10	H1.97	I/O	•	Not connected.	
USER11	H1.99	I/O	•	Not connected.	

PPM PIN DESCRIPTIONS – User-defined

SERIAL FLASH MEMORY INTERFACE

PPM D1 has an external 64Mbit serial flash memory (SFM) peripheral implemented via an SPI interface to an Atmel AT25DF641 (U5). The preferred method of interfacing to U5 is by using U1's third SPI interface (SPI3) — this will permit a very high-speed interface to U5. The pin assignments associated with this interface are listed below.

If the user desires to map SPI3 to the PPM connector instead, the SFM interface pins can be configured as simple I/O, using a software SPI driver to read and write from/to the SFM.

Name	Pin	I/O	Description		
-WP	U5.3	I/O	-WP_SFM. SFM write-protect function. From RD6 (U1.83). Part of the third		
-WE	-WP 05.3		SPI interface. RD6 is normally configured as a simple output.		
-cs U5.1	U5.1	I/O	-CS_SFM. SFM chip select. From RD13 (U1.80). Part of the third SPI		
-05	05.1	1/0	interface. RD13 is normally configured as a simple output.		
SDT I	U5.5	I/O	SDO_SFM. SPI2 (master) data out. From RP11 (U1.72). Part of the third		
SDI	SDI 05.5 1/	1/0	SPI interface. RP11 is normally configured as output function SDO3.		
SDO		I/O	SDI_SFM. SPI2 (master) data in. From RP3 (U1.70). Part of the third SPI		
500 05.2	U5.2		interface. RP3 is normally configured as input function SDI3.		
SCK	U5.6	I/O	SCK_SFM. SPI2 clock. From RP12 (U1.71). Part of the third SPI interface.		
SCK	05.0		RP12 is normally configured as output function SCK3OUT.		

PIN DESCRIPTIONS – Serial Flash Memory Interface

CONNECTORS

Item	Description	Source	Part Number	Application
1	100-pin, hermaphroditic	Samtec	LSS-150-01-L-DV	PPM connector (standard, +3mm)

This connector information is provided for reference only.

PROGRAMMING & DEBUGGING

PPM D1 provides two interfaces for programming and debugging – the popular and low-cost In-Circuit Debugging (ICD) interface, and a JTAG interface. Both are implemented via Flexible Printed Circuit (FPC) connectors on the PPM.

6-pin FPC connector **J1** is for the ICD. Via Pumpkin's JFPC-PIC24 adapter, customers can connect either a traditional Microchip® ICD like the ICD2, with its 6-pin RJ11 6P6C connector⁶, or a Microchip PICKit, with its 6-pin 0.100" pitch in-line header. The JFPC-PIC24 connects to PPM D1 via a 6-conductor

⁶ Also called RJ25.

FPC cable. **PGEC** (U1.24) and **PGED** (U1.25) are used as the clock/data pair for the ICD. No isolation from these signals to the CSK bus is provided – therefore care should be taken in connecting circuitry to IO.36 and IO.37 of the CSK bus.

8-pin FPC connector **J2** is for JTAG, and is compatible with 8-conductor FPC cables. Customers who wish to use the JTAG port must fabricate their own adapter.

NOTES

The PIC24's Peripheral Pin Select system enables the user to place digital peripherals at the selected I/O pins of choice. On PPM D1, the peripheral functions (e.g., second and third I2C interfaces, second SPI interface, third and fourth UART interfaces) beyond those that interact with peripheral hardware on the MB have been arranged in a logical manner on the PPM connector, and will correspond to the same arrangement on other PPMs where such additional peripherals present in the processor utilized on that PPM.

Additionally, some mappable peripherals (e.g., the third and fourth UARTs) are not assigned pins on the PPM connector. The user can bring them to the CubeSat Kit bus – and thereby to any CubeSat Kit-compatible modules – by mapping them to unused RP/RPI pins (e.g., those on IO.16 through IO.19), or to other RP/RPI pins of choice. In all cases, IO.0 through IO.7 should remain with the peripheral assignments outlined above, as they correspond to resources on the CSK MB.

PPM D1 (PIC24) is built on the same Pumpkin PCB (705-00525) as PPM D2 (dsPIC33), with minor differences in the components placed at assembly time.

TRADEMARKS

The following are Pumpkin trademarks. All other names are the property of their respective owners.

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