http://www.cubesatkit.com/

CubeSat Kit™ Motherboard Module (MBM) 2

Hardware Revision: E

Motherboard for BeagleBone Black (BBB)

ORDERING INFORMATION

Pumpkin P/N 710-01362

Option Code	CubeSat Kit Bus Connector
/00 (standard)	stackthrough
/01	non-stackthrough

Contact factory for availability of optional configurations. Option code /00 shown.

CAUTION

Electrostatic Sensitive Devices

Handle with Care

Applications

- CubeSat nanosatellites
- SUPERNOVA™ nanosatellites

Features

- For use with 104-pin CubeSat Kit™ Bus
- Hosts BeagleBone Black (BBB) as a single 0.600” tall CSK-compatible module
- Multiple +5V power sources supported, auto-selected
- BBB Ethernet, USB host & USB device ports fully supported
- BBB 4.5x UART, 1x I2C & 6x GPIO mapped to CSK Bus Connector
- RS-422 + LVTTL SPI/UART/GPIO PHY for transceivers
- BBB UART0 breakout
- Power-on fully protected I/O
- On-board reset circuitry, drives BBB’s **SYS_RESETn** and GPIO buffers
- On-board SD Card interface (SPI mode)
- On-board Real-Time Clock (RTC) with battery backup
- On-board **–RESET** & **OFF_VCC**-driven WDT interface
- Independent latchup (device overcurrent) protection on critical subsystems
- PC/104-size footprint
- Stackable 104-pin CubeSat Kit Bus connectors includes processor’s complete I/O space, user-assignable signals and more
- Wiring-free module interconnect scheme
- 4-layer gold-plated blue-soldermask PCB with ground plane for enhanced signal integrity

December 2017 – document Rev. A

CHANGELOG

Rev.	Date	Author	Comments
A	20171221	AEK	Initial release of hardware Rev E.

OPERATIONAL DESCRIPTION

The Motherboard Module 2 is a CubeSat Kit (CSK)-compatible host for the COTS BeagleBone Black (BBB) Rev C and compatible variants thereof. When installed onto an MBM 2, the BBB interfaces to the CSK electrical bus via standardized signals. Additional features like a Real-Time Clock (RTC) with battery backup and a full-size SD Card operating in SPI mode are also provided.

Power-on and reset behavior of the combined MBM 2 + BBB is carefully controlled to ensure proper operation and protection of BBB I/O when interfacing to other modules through the CSK bus connector. This is accomplished via high-speed, zero-power level-shifter / isolators between the BB and the CSK bus connector. The isolators are disabled while the BBB is in reset, and are enabled once the BBB comes out of reset and is ready to handle signals at its I/O pins. This protection prevents non-phased power sequencing within the CSK architecture from damaging the BBB's I/O.[1]

Four and a half UARTs (two with -CTS/-RTS flow control), one SPI, one I2C, five general-purpose outputs and one general-purpose input are mapped between the BBB and the CSK bus connector. Additionally, seven dedicated analog inputs are mapped from the CSK bus connector to the BBB's analog inputs.

BBB Signal	Description	CSK Signal
UART1_RXD	BBB UART 1 receive	The "second" CSK UART (Ux1), with flow control. Historically, this serial channel has been used to communicate with a radio / modem.
UART1_TXD	BBB UART 1 transmit	
UART1_RTSn	BBB UART 1 flow control	
UART1_CTSn	BBB UART 1 flow control	
UART2_RXD	BBB UART 2 receive	The "third" CSK UART (Ux2), without flow control. Historically, this serial channel has been used to communicate with a GPS receiver and/or other serial devices.
UART2_TXD	BBB UART 2 transmit	
UART3_TXD	BBB UART 3 transmit	The "fifth" CSK UART (Ux4), transmit only.
UART4_RXD	BBB UART 4 receive	The "fourth" CSK UART (Ux3), without flow control. Historically, this serial channel has been used to communicate with a GPS receiver and/or other serial devices.
UART4_TXD	BBB UART 4 transmit	
UART5_RXD	BBB UART 5 receive	The "first" CSK UART (Ux0), with flow control. Historically, this serial channel has been used to communicate with an ADACS.
UART5_TXD	BBB UART 5 transmit	
UART5_RTSn	BBB UART 5 flow control	
UART5_CTSn	BBB UART 5 flow control	
SPI1_SCLK	BBB SPI 1 interface	The "first" CSK SPI (SPI0). Historically, this interface has been used to communicate with an SD card hosting a FAT filesystem.
SPI1_DO		
SPI1_DI		
SPI1_CS0		
GPIO2_22	BBB general-purpose output	General-purpose output
GPIO2_23		
GPIO2_24		
GPIO2_25		
GPIO2_1	BBB general-purpose input	General-purpose input
I2C1_SDA	BBB I2C data	The "first" I2C. Historically, this interface has been used to communicate with various subsystems.
I2C1_SCL	BBB I2C clock	
AN6 – AN0	BBB AIN6-AIN0 analog inputs	Analog inputs to the host (BBB)
AN7		-BUFF_EN, indicates when active that the BBB's I/O is actively connected to the CSK Bus Connector

Table 1: MBM 2 BBB-to-CSK bus connector digital signal mappings

BBB features that remain untouched and that can be used independently of the CSK bus connector include:

- Ethernet (via 100BaseT / RJ45)
- USB host (via USB type A)
- USB device (via USB micro-B)
- HDMI (via micro-HDMI)
- SD card (via micro-SD socket)
- COM0/UART0 (via 1x6 SIP header)
- External +5Vdc power (via 2.1/5.5mm barrel jack)

[1] The I/O protection afforded by the MBM 2's I/O isolators applies only to digital I/O. The BBB's analog inputs are connected directly to the BBB's analog input pins. Users should control analog inputs to the BBB via the **-BUFF_EN** output signal.

Additionally, several signals are mapped from the BBB and MBM 2 to a dedicated Omnetics® BiLobe 25-pin connector that is used as a physical interface (PHY) to a high-speed module.

Signal Name	BBB Signal	Interface / Level	Notes
PHY_XMT0+	SPI1_DO or UART0_TXD	RS-422 with configurable series and/or and parallel termination. Uses TI SN65HVD73 (20Mbps) RS-485 transceivers.	Typically used as part of a 4-wire SPI interface using SPI1. A chip select signal other than the BBB's –CS0 may be required. This SPI is shared with the SPI-based SD Card. Alternatively, can be configured as an RS-422 UART and a GPIO pair. No UART peripheral CTS/RTS signals are supported in this configuration.
PHY_XMT0–			
PHY_XMT1+	SPI1_SCLK		
PHY_XMT1–			
PHY_RCV0+	SPI1_DI or UART0_RXD		
PHY_RCV0–			
PHY_RCV1+	GPIO1_28		
PHY_RCV1–			
PHY_XMT2	GPIO2_9	3.3V LVTTL	Typically used as (single-ended) –CS for RS-422 PHY
PHY_XMT3	GPIO2_10		Typically used to augment the RS-422 PHY via slower GPIO signals.
PHY_XMT4	GPIO2_11		
PHY_RCV2	GPIO2_12		
PHY_RCV3	GPIO2_13		
PHY_RXD	UART0_TXD		The BBB's UART0 can be connected to a remote device.
PHY_TXD	UART0_RXD		
SDA_SYS	I2C1_SDA	Pulled up to 3.3V on MBM 2.	
SCL_SYS	I2C1_SDA		

Table 2: MBM 2 PHY connector signal mappings

An external watchdog timer (WDT) interface is provided.

The BBB operates from system +5Vdc power (**+5V_SYS**). BBB I/O (and therefore its I/O signals on the BBB bus connector) operates at +3.3V logic levels.

Note that unlike other Pumpkin Pluggable Processor Modules (PPMs) with general-purpose I/O mapped to the CSK bus connector, the MBM 2 provides unidirectional signals (and power-on sequencing and protection) between the BBB and the CSK bus connector, on a per-GPIO-pin basis. Also, note that not all of the BBB's **P8** and **P9** pins are mapped to the CSK bus connector. Future revisions of the MBM 2 may map additional BBB pins to the CSK bus connector, and/or may allow for bidirectional digital I/O signals.

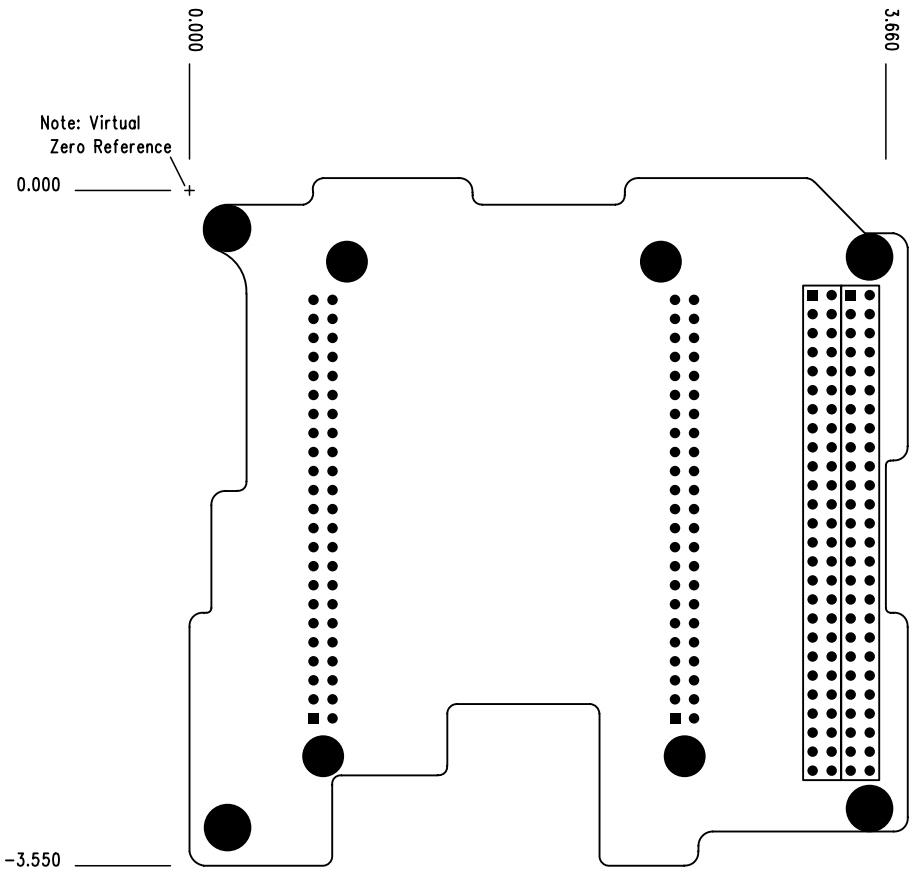
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature	T_A	-40 to +85	ºC
Voltage on **+5V_USB** bus		-0.3 to +6	V
Voltage on **+5V_SYS** bus			
Voltage on **VCC_SYS** bus		-0.3 to +3.6	V
Voltage on local **VCC** bus			

PHYSICAL CHARACTERISTICS

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Mass				31		g
Height of components above PCB					11	mm
Height of components below PCB	Not including stacking H1/H2 connectors				3.5	mm
PCB width	Corner hole pattern matches PC/104			96		mm
PCB length				90		mm
PCB thickness				1.6		mm
CubeSat Kit Bus Connector terminal pitch	Horizontal or vertical distance to nearest terminal			2.54		mm
Pumpkin PCB P/N		705-01168				

SIMPLIFIED MECHANICAL LAYOUT [2]



[2] Dimensions in inches.

ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

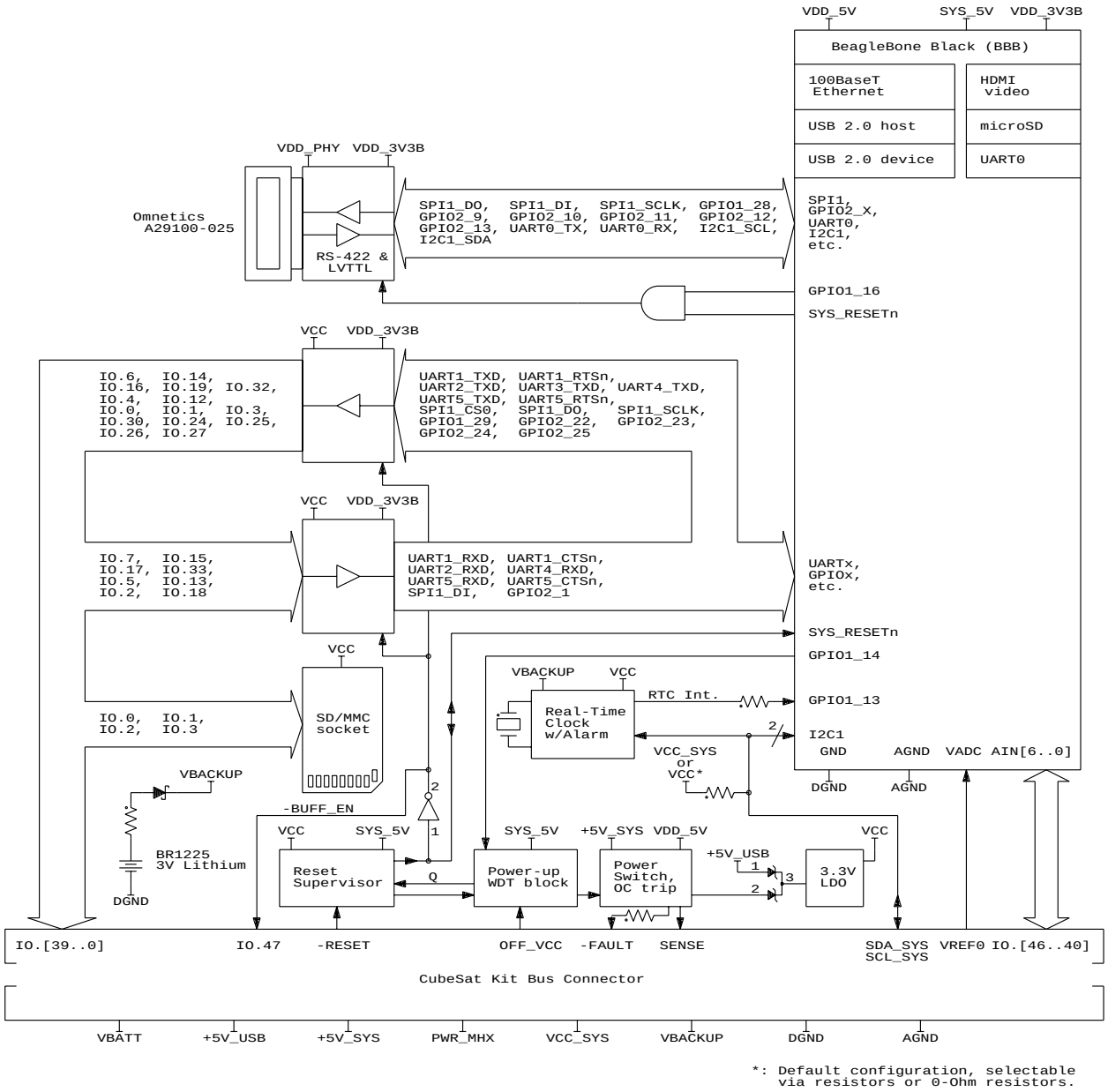
Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Maximum external dc voltage on **+5V_SYS** or to **P1** on BBB	Overvoltage will damage MBM 2 and/or BBB	$V_{+5V\_IN\_MAX}$			6.0	V
Backup battery voltage	Feeds **VBACKUP** through **R20** (4.7kΩ).	V_{BT1}		3.0	3.5	V
Operating current (exclusively from **+5V_SYS**)	Without BBB	$I_{OP\_NO\_BBB}$		10		mA
	With BBB, Ethernet disabled	$I_{OP\_BBB\_NO\_ETH}$		300		mA
	With BBB, Ethernet enabled	$I_{OP\_BBB\_ETH}$		350		mA
RTC crystal frequency	No external capacitors	f_{CLK_RTC}		32.768 ± 0.001		kHz
Overcurrent trip point for **VDD_5V**	Set by **R1**	I_{TRIP_5V}		920		mA
Overcurrent trip point for **+5V_USB**	Set by **R14**	I_{TRIP_USB}		750		mA
Data rate through any on-board isolator (**U1**-**U3**)			50			MHz

Parameter	Conditions / Notes	Min	Typ	Max	Units
I2C addresses available to slave devices	Set by BBB (I2C Master, 7-bit addresses)		0x04-0x7F		
I2C clock speed			400		kHz
I2C pull-up resistors	Pull-up resistors **R83** & **R84**[3,4]		1.5k		Ω

[3] Default value. Users should evaluate the I2C bus performance in their particular application and replace these resistors with optimal values.

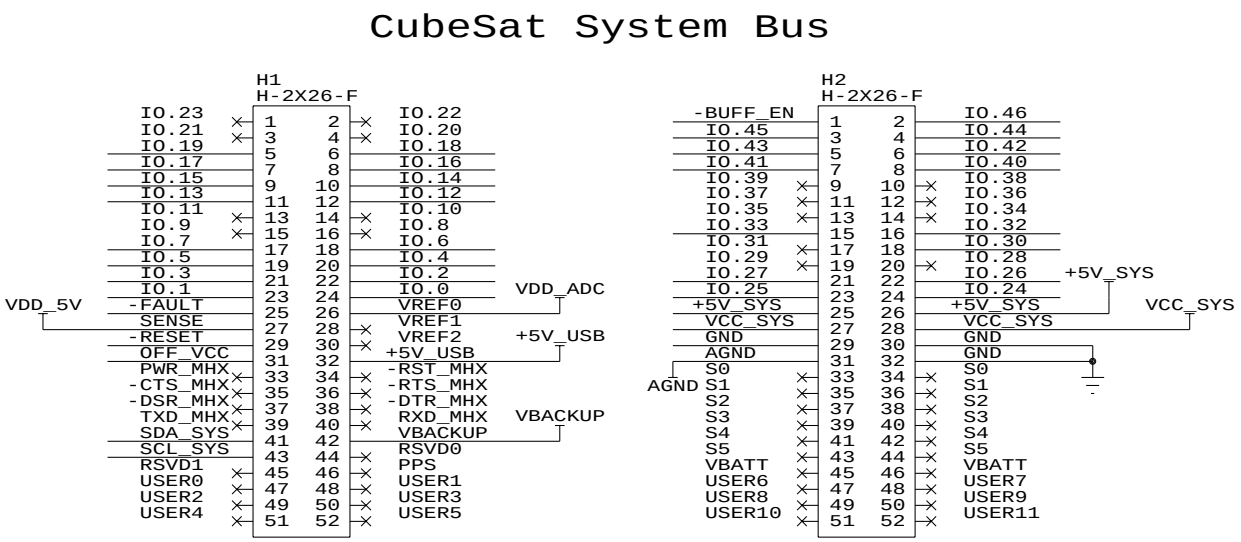
[4] The MBM 2 supports pull-ups to two different voltage sources (local **VCC** and **VCC_SYS**). Consult the MBM 2 schematics for more information.

BLOCK DIAGRAM



*: Default configuration, selectable via resistors or 0-Ohm resistors.

CubeSat Kit Bus PIN DESCRIPTIONS



CubeSat Kit Bus PIN DESCRIPTIONS – I/O

Name	Pin	I/O	Description
IO.0	H1.24	O	**-CS_SD**. Controls SD Card interface. *Part of the MBM 2's SD card interface. Output from the BBB's SPI1_CS0.*
IO.1	H1.23	O	**SDO**. SPI master data out. *Part of the MBM 2's SD card interface. Output from the BBB's SPI1_DO.*
IO.2	H1.22	I	**SDI0**. SPI master data in. *Part of the MBM 2's SD card interface. Input to the BBB's SPI1_DI.*
IO.3	H1.21	O	**SCK0**. SPI clock. *Part of the MBM 2's SD card interface. Output from the BBB's SPI1_SCLK.*
IO.4	H1.20	O	**UTX0**. Serial data out at +3.3V logic levels. *Output from the BBB's UART5_TXD.*
IO.5	H1.19	I	**URX0**. Serial data in at +3.3V logic levels. *Input to the BBB's UART5_RXD.*
IO.6	H1.18	O	**UTX1**. Serial data out at +3.3V logic levels. *Output from the BBB's UART1_TXD.*
IO.7	H1.17	I	**URX1**. Serial data in at +3.3V logic levels. *Input to the BBB's UART1_RXD.*
IO.8	H1.16		Not connected.
IO.9	H1.15		Not connected.
IO.10	H1.14		Not connected.
IO.11	H1.13		Not connected.
IO.12	H1.12	O	**-URTS0**. Request-to-send (RTS) serial handshake at +3.3V logic levels, active low. *Output from the BBB's UART5_RTSn.*
IO.13	H1.11	I	**-UCTS0**. Clear-to-send (CTS) serial handshake at +3.3V logic levels, active low. *Input to the BBB's UART5_CTSn.*
IO.14	H1.10	O	**-URTS1**. Request-to-send (RTS) serial handshake at +3.3V logic levels, active low. *Output from the BBB's UART1_RTSn.*
IO.15	H1.9	I	**-UCTS1**. Clear-to-send (CTS) serial handshake at +3.3V logic levels, active low. *Input to the BBB's UART1_CTSn.*
IO.16	H1.8	O	**UTX2**. Serial data out at +3.3V logic levels. *Output from the BBB's UART2_TXD.*
IO.17	H1.7	I	**URX2**. Serial data in at +3.3V logic levels. *Input to the BBB's UART2_RXD.*
IO.18	H1.6	I	General-purpose input. *Input to the BBB's GPIO2_1.*
IO.19	H1.5	O	**UTX4**. Serial data out at +3.3V logic levels. *Output from the BBB's UART3_TXD.*
IO.20	H1.4		Not connected.
IO.21	H1.3		Not connected.

IO.22	H1.2		Not connected.
IO.23	H1.1		Not connected.
IO.24	H2.24	O	General-purpose output. *Output from BBB's GIPO2_22.*
IO.25	H2.23	O	General-purpose output. *Output from BBB's GIPO2_23.*
IO.26	H2.22	O	General-purpose output. *Output from BBB's GIPO2_24.*
IO.27	H2.21	O	General-purpose output. *Output from BBB's GIPO2_25.*
IO.28	H2.20		Not connected.
IO.29	H2.19		Not connected.
IO.30	H2.18	O	General-purpose output. *Output from BBB's GIPO1_29.*
IO.31	H2.17		Not connected.
IO.32	H2.16	O	**UTX3**. Serial data out at +3.3V logic levels. *Output from the BBB's UART4_TXD.*
IO.33	H2.15	I	**URX3**. Serial data in at +3.3V logic levels. *Input to the BBB's UART4_RXD.*
IO.34	H2.14		Not connected.
IO.35	H2.13		Not connected.
IO.36	H2.12		Not connected.
IO.37	H2.11		Not connected.
IO.38	H2.10		Not connected.
IO.39	H2.9		Not connected.
IO.40	H2.8	I	**AN0** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN0.*
IO.41	H2.7	I	**AN1** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN1.*
IO.42	H2.6	I	**AN2** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN2.*
IO.43	H2.5	I	**AN3** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN3.*
IO.44	H2.4	I	**AN4** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN4.*
IO.45	H2.3	I	**AN5** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN5.*
IO.46	H2.2	I	**AN6** analog input at maximum +3.3Vdc. *Direct input to BBB's AIN6.*
IO.47	H2.1	O	**-BUFF_EN**. *When high (+3.3V), indicates that BBB's I/O is in a high-impedance state relative to the CSK bus connector. When low (0V), indicates that BBB's I/O to the CSK bus connector is active.*

CubeSat Kit Bus PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	Description
VREF0	H1.26	I	ADC reference voltage. *Connected to BBB's **VDD_ADC**. Provides the positive reference voltage for the BBB's ADC system.*
VREF1	H1.28		Not connected.
VREF2	H1.30		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	Description
RSVD0	H1.44	–	Not connected.
RSVD1	H1.45	–	Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	Description
SDA_SYS	H1.41	I/O	I2C data. *From/to the BBB's I2C1_SDA.*
SCL_SYS	H1.43	O	I2C clock. *From the BBB's I2C1_SCL.*

CubeSat Kit Bus PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	Description
-FAULT	H1.25	O	Open-collector output from MBM 2's latchup-prevention overcurrent switch. Active LOW. Wire-ORed signal.
SENSE	H1.27	–	Current sense signal. *Can be used to measure MBM 2's + BBB's current consumption. The current drawn from **+5V_SYS** is (**+5V_SYS** – **SENSE**) / 75mΩ.*
-RESET	H1.29	I/O	Input to reset supervisor. Output from MBM 2 if **SW1** is fitted (non-default). *An active signal (0Vdc) on this input will reset the BBB if/when the BBB has enabled its bus reset input via GPIO1_14.*
OFF_VCC	H1.31	I	Input to latchup-prevention overcurrent switch. Output from MBM 2 if **SW1** is fitted (non-default). *An active signal (+5Vdc) on this input will disable **+5V_SYS** power to the BBB if/when the BBB has enabled its bus reset input via GPIO1_14.*
PPS	H1.46		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – RBF and Separation Switches

Name	Pin	I/O	Description
S0	H2.33 H2.34		Not connected.
S1	H2.35 H2.36		Not connected.
S2	H2.37 H2.38		Not connected.
S3	H2.39 H2.40		Not connected.
S4	H2.41 H2.42		Not connected.
S5	H2.43 H2.44		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – Power

Name	Pin	I/O	Description
VBATT	H2.45 H2.46		Not connected.
+5V_USB	H1.32	I/O	+5V USB power. From USB host. Powers local circuitry.
+5V_SYS	H2.25 H2.26	I	+5V system power. Powers the BBB and local circuitry.
PWR_MHX	H1.33		Not connected.
VBACKUP	H1.42	O	Battery backup voltage (e.g. for RTC). *From MBM 2's 3V Lithium battery **BT1**.*
VCC_SYS	H2.27 H2.28	I	VCC System power. Assumed to be +3.3V. Used only as a configurable pull-up voltage for I2C.
AGND	H2.31	I	Analog ground. *Connected to BBB's **GNDA_ADC**. Provides the negative reference voltage for the BBB's ADC system.*
DGND	H2.29 H2.30 H2.32	–	Digital ground.

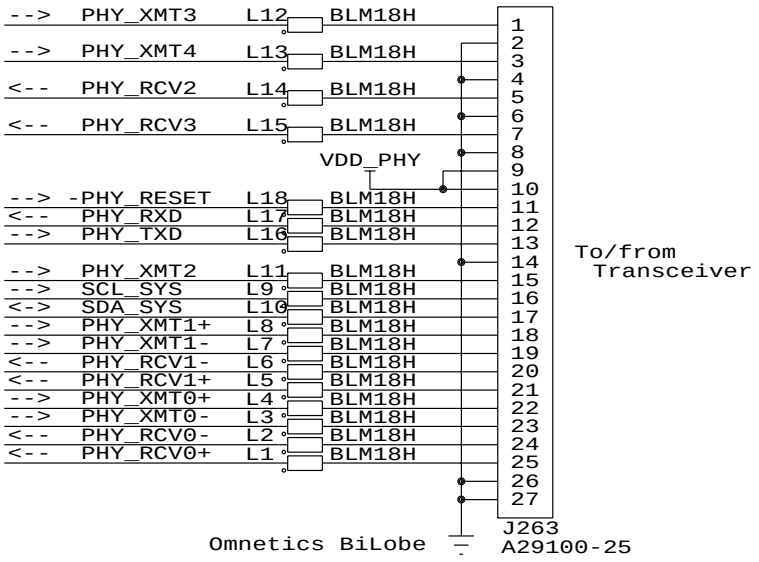
CubeSat Kit Bus PIN DESCRIPTIONS – Transceiver Interface

Name	Pin	I/O	Description
-RST_MHX	H1.34		Not connected.
-CTS_MHX	H1.35		Not connected.
-RTS_MHX	H1.36		Not connected.
-DSR_MHX	H1.37		Not connected.
-DTR_MHX	H1.38		Not connected.
TXD_MHX	H1.39		Not connected.
RXD_MHX	H1.40		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	Description
USER0	H1.47		Not connected.
USER1	H1.48		Not connected.
USER2	H1.49		Not connected.
USER3	H1.50		Not connected.
USER4	H1.51		Not connected.
USER5	H1.52		Not connected.
USER6	H2.47		Not connected.
USER7	H2.48		Not connected.
USER8	H2.49		Not connected.
USER9	H2.50		Not connected.
USER10	H2.51		Not connected.
USER11	H2.52		Not connected.

PHY PIN DESCRIPTIONS



PHY PIN DESCRIPTIONS – Transceiver Interface

Name	Pin	I/O	RS-422	3.3V LVTTL	Description
PHY_XMT3	J263.1	O		●	User-defined. From **GPIO2_10**.
GND	J263.2				
PHY_XMT4	J263.3	O		●	User-defined. From **GPIO2_11**.
GND	J263.4				
PHY_RCV2	J263.5	I		●	User-defined. To **GPIO2_12**.
GND	J263.6				
PHY_RCV3	J263.7	I		●	User-defined. To **GPIO2_13**.
GND	J263.8				
VDD_PHY	J263.9 J263.10				Configurable as +5V or +3.3V. Enabled when BBB's **SYS_RESETn** is inactive/HIGH and **GPIO1_16** is active/HIGH.
-PHY_RESET	J263.11	O			When configured, tied to **–RESET** via an RC filter.
PHY_RXD	J263.12	I		●	Serial input to BBB.
PHY_TXD	J263.13	O		●	Serial output from BBB.
GND	J263.14				
PHY_XMT2	J263.15	O		●	User-defined. From **GPIO2_9**.
SCL_SYS	J263.16	O			From/to I2C signals on CSK connector.
SDA_SYS	J263.17	I/O			
PHY_XMT1+	J263.18	O	●		From **SPI1_SCLK**.
PHY_XMT1-	J263.19				
PHY_RCV1-	J263.20	I	●		To **GPIO1_28**.
PHY_RCV1+	J263.21				
PHY_XMT0+	J263.22	O	●		From **SPI1_DO** or **UART0_TXD**.
PHY_XMT0-	J263.23				
PHY_RCV0-	J263.24	I	●		To **SPI1_DI** or **UART0_RXD**.
PHY_RCV0+	J263.25				

Compatibility

MBM 2 has been tested with and is intended for use with the following instances of the open-source BeagleBone Black design:[5]

Manufacturer	Product Name / ID	Supported?	Notes
CircuitCo, LLC	BeagleBone Black	yes	Rev C. Digi-Key® P/N BB-BBLK-000-REVC-ND[6]
Element 14	BeagleBone Black	no	

Power

The MBM 2 draws its power from the CSK's **+5V_SYS** and/or **+5V_USB**, and uses the resultant +5Vdc power to generate a local 3.3V (**VCC**) as well as to power the BBB at +5Vdc. +5Vdc power drawn from **+5V_SYS** is current-limited and will automatically trip and reset if the setpoint is exceeded. **VCC** is used to drive peripherals on the MBM 2 (e.g., RTC and SD Card) and to establish the I/O voltage level for the BBB.

+5Vdc power can also be applied (at any time) via the BBB's barrel jack connector P1 and/or its mini-USB device connector.[7] The various power possibilities are shown below. The BBB is on whenever a +5V power source (internal or external) is connected to the MBM 2 + BBB.

Bus power enabled	USB Host connected	External +5V power input at P1	+5V_SYS power	+5V_USB power	BBB status
			off	off	off
●			on	off	on
		●	off	off	on
●		●	on	off	on
	●	●	off	off	on
	●		off	on	on
●	●		on	on	on
●	●	●	on	on	on

Table 3: System & BBB power status based on +5V power sources

Logic-level Interfacing to the BBB

The BBB's I/O operates at +3.3V LVTTL levels, referenced to the BBB's **VDD_3V3B** power bus.

All of the push-pull GPIO signals from the BBB to the CSK bus connector pass through unidirectional isolators on the MBM 2 and present themselves as CSK bus signals at LVTTL signals referenced to local **VCC** (normally +3.3V). These isolators are enabled only when the BBB's bidirectional **SYS_RESETn** signal is inactive, i.e. the BBB is no longer in reset. An inverted, unidirectional version of **SYS_RESETn** is provided as the **–BUFF_EN** output on the CSK bus connector.

When interfacing to any of the BBB's signals mapped to the CSK bus connectors **IO.[39..0]** signals, note that all are inactive / high-impedance until **–BUFF_EN** is active. Based on warnings included with each BBB, it's possible that the prohibition on connecting any signals to the BBB's inputs before its has come out of reset also applies to the analog inputs **AIN[6..0]**; the **–BUFF_EN** signal can be used to gate analog signals that connect to **AIN[6..0]**.

BBB open-collector / open-drain signals like I2C1's **SDA** and **SCL** signals are connected directly to the CSK bus connector; no isolators are involved.

[5] See beagleboard.org for more information.

[6] It's unclear whether this Digi-Key part number is a generic one for all Rev C BeagleBone Blacks, or just the ones from CircuitCo.

[7] This assumes that the EPS connected to the CSK bus connector can handle external +5V power sources on **+5V_SYS**. This is often true.

PHY Transceiver Interface

The PHY consists of four RS-422 signals (2 Rx & 2 Tx), five 3.3V LVTTL signals (3 Tx & 2 Rx), UART0 at 3.3V LVTTL or RS-422 levels, the system I2C bus, and power, ground and a reset signal. This PHY interface is power-on-reset protected, and is enabled only when **GPIO1_16** is active/HIGH and the BBB's **SYS_RESETn** signal is inactive/HIGH.

A configurable 5V/3.3V power source **VDD_PHY** is available. It is primarily intended to provide power for any active circuitry or other powered electronics on the other end of the interface.

Some of the signals on the PHY transceiver interface can be configured at the factory. For example, the first **PHY_XMT/RCV** RS-422 signal pair can be configured as **SPI1_DO/DI** or **UART0_TX/RX**. Similarly, the LVTTL **UART0_TX/RX** pair can be omitted, as can the I2C **SCL_SYS/SDA_SYS** pair. Contact the factory for more information.

An example configuration for the PHY transceiver interface is shown below. This is for a high-speed RF transceiver that has an SPI interface as its high-speed data interface, and several GPIO signals for lower-speed signaling.

Signal Name		Direction	Signal Function
MBM 2	PHY		
PHY_XMT0	SPI_MOSI	BBB → PHY	RS-422 SPI data out to transceiver
PHY_RCV0	SPI_MISO	BBB ← PHY	RS-422 SPI data in from transceiver
PHY_XMT1	SPI_SCLK	BBB → PHY	RS-422 SPI clock
PHY_RCV1	SPI_RDY	BBB ← PHY	RS-422 SPI ready from transceiver
PHY_XMT2	SPI_FS	BBB → PHY	LVTTL SPI chip select
PHY_XMT3	SelProgSW_0	BBB → PHY	LVTTL Firmware select bit 0
PHY_XMT4	SelProgSW_1	BBB → PHY	LVTTL Firmware select bit 0
PHY_RCV2	RcvState_0	BBB ← PHY	LVTTL Receive state indicator bit 0
PHY_RCV3	RcvState_1	BBB ← PHY	LVTTL Receive state indicator bit 1
SCL_SYS	I2C_SCL	BBB → PHY	I2C clock
SDA_SYS	I2C_SDA	BBB ←→ PHY	I2C data
PHY_TXD		BBB → PHY	Not used
PHY_RXD		BBB ← PHY	
-PHY_RESET		BBB → PHY	
VDD_PHY			

Table 4: Sample signal functions for 25-pin PHY interface

The PHY transceiver connector on the MBM 2 is an Omnetics A29100-025. A mating, straight-through 18"/457mm harness is Omnetics A42631-025.

Reset Supervisor

A local reset supervisor is provided. Its output is gated through the WDT interface (below) and is used to establish the power-on state of the power-up WDT block. An user-supplied pushbutton switch can be fitted to the MBM 2 to enable manual resets of the BBB.[8]

Watchdog Timer Interface

The MBM 2 supports an external watchdog timer (WDT) that controls the system **–RESET** and/or **OFF_VCC** signals. At power-on and whenever **–RESET** is active, the BBB is isolated from the effects of the **–RESET** and **OFF_VCC** signals via a dedicated WDT interface; this allows the BBB to use its own local power-on/reset circuitry get through boot-up and other actions whose time-to-complete may exceed the external WDT's period. To allow external bus signals to reset and/or power-cycle the BBB, the BBB must explicitly clock the local **GPIO1_14** signal[9] low-to-high at least once. This low-to-high transition unblocks

[8] The BBB has its own reset button, though it is hard to reach when the BBB is mounted to the MBM 2.

[9] **GPIO1_14** is pulled down on the MBM 2.

the **-RESET** and **OFF_VCC** signals so that when active, they can reset and power-down the BBB, respectively. Once the WDT interface is unblocked, the active-low **-RESET** signal will hold the BBB in reset as long as it is active, and the active-high **OFF_VCC** signal will power-down the BBB and the MBM 2 as long as it is active. The MBM 2's WDT interface will remain in this state until a reset or system power-cycling event on **+5V_SYS**.

The off-board external WDT should be configured to drive **–RESET** and/or **OFF_VCC** active when the BBB has failed to kick the watchdog correctly. Typically, a GPIO output from the BBB to the external WDT is used to kick the WDT.

When the MBM 2 is powered via USB, the **OFF_VCC** signal is effectively disabled on the MBM 2, and cannot power-cycle the BBB. The ability to reset the BBB via external WDT control of the **–RESET** signals remains.

SD Card Interface

An SD Card socket provides a 4-wire, SPI-mode SD Card interface to the BBB's **SPI1_CS0**, **SPI1_DO**, **SPI1_DI** and **SPI1_SCLK** signals. The SD Card socket is connected directly to the CSK bus connector's **IO.[3..0]** signals; therefore, it can be accessed by other devices as long as the chip select signal **IO.0** driven by the BBB's **SPI1_CS0** is under organized / arbitrated control.

The SD Card is powered from the local **VCC** (+3.3V).

The signal lines between the SD card and the BBB have no series resistors; therefore SPI clock speeds in the 20-50MHz range are possible, as long as they are supported by the SD Card.

Real-Time Clock

The 8-pin M41T81S RTC on the MBM 2 functions as a slave I2C device and is connected directly to the CSK I2C bus (**SDA_SYS** & **SCL_SYS**); no I2C isolator is employed. A 3V Lithium coin-cell battery holder is present on the MBM 2; when fitted, the **VBACKUP** power bus provides current-limited backup power to the RTC for the purpose of maintaining a real-time clock even when other power sources (**+5V_SYS**, **VCC_SYS**, etc.) are not present.

Backup Battery

The MB has a replaceable BR1225 3V Lithium coin cell to serve as a backup battery **BT1** for real-time clocks and other components requiring battery backup of volatile information.

Battery **BT1** is held in place by a coin cell battery holder in one corner of the underside of the MB. The all-metal battery holder is oriented in such a way that once installed onto a CubeSat Kit Base Plate, the battery cannot slide out of its battery holder and is thereby physically restrained along five of six axes. However, since the battery has a conductive outer shell, excessive movement of the battery along its insertion / removal axis could result in a short if it were to contact the Base Plate. Therefore insulating Kapton tape and/or an epoxy or silicone adhesive should be applied to the battery and battery holder.

Alternately, the customer can feed **VBACKUP** on the CubeSat Kit bus via their own backup battery located elsewhere in the system.

I2C

The BBB on the MBM 2 normally functions as an I2C master controller on the BBB's **I2C1** interface.

By default, I2C pull-ups of 1.5kΩ are connected to the MBM 2's local **VCC** supply (+3.3V). Optionally, they can be connected to **VCC_SYS** (+3.3Vdc). See the MBM 2 schematics for more information.

The MBM 2 does not utilize the BBB's I2C0 (the I2C bus used for control interface, etc.). It remains free for the BBB to use locally.

The MBM 2 does not utilize the BBB's I2C2 (the I2C bus used for Cape identification and enumeration). While I2C2 is pinned out on the BBB's P9, it overlaps the BBB's **UART1_RTSn** and **UART1_CTSn** signals. These signals pass through unidirectional isolators on their way to the CSK bus connector. Therefore I2C2 is not available on the CSK bus connector, even if the flow control features of the BBB's UART1 are not used.

BBB Cape Support

Because the BBB is mounted "upside-down" on the MBM 2 (i.e., the mating connectors for the BBB's P8 and P9 are male headers on the MBM 2), and because of the I2C2–UART1 flow control overlap (see above), it is not possible to use standard BBB-compatible Capes with the MBM 2 + BBB.

BBB Analog Inputs

All seven of the BBB's dedicated analog inputs **AIN[6..0]** are mapped to the CSK bus connector signals **AN[6..0]**. The reference voltage for the BBB's ADC (**VDD_ADC**) is mapped to the CSK bus connector signal **VREF0**; an external reference voltage can be provided via this input. Care must be exercised when applying analog voltages to the BBB if/when the BBB is in reset – see Logic-level Interfacing to the BBB, above.

Fitment

The BBB is affixed to the MBM 2 via four custom aluminum spacers. A combined heatsink/spacer is available from the factory.

In some instances, the overall height of the module may be incompatible with certain stackups within a nanosatellite that expects to stack modules utilizing the standard 0.600" board-to-board spacing. In these situations, it may be necessary to trim the **P8** and **P9** header pins on the underside of the MBM 2. It may also be necessary to remove some (unused) connectors of the BBB, e.g. the HDMI connector.

RBF and Separation Switches

The MBM 2 does not support RBF or Separation Switches – they must be accommodated elsewhere if/when required.

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