CubeSat Kit™
Electrical Power System Module 1 (EPSM1)

Hardware Revision: C

http://www.cubesatkit.com/

High-power, high-efficiency multi-channel spacecraft power system

Applications

- CubeSats & nanosatellites
- Pumpkin MISC™ 3 CubeSats
- Pumpkin SUPERNOVA™ NanoSats
- Difficult loads (e.g., cryocoolers)

Features

- SWaP:
  - < 0.2U, < 300g, < 3W
- 96-98.5% efficient 250kHz GaNFET switching
- SEU-Immune power control FPGA
- 32V power ring topology with:
  - 6 solar array inputs (8-28V, 2A/4A)
  - 2 battery (16.8V, 8A) blocks
  - 3 regulated outputs (3.3/5.0/12V, 5-8A)
  - 1 switchable regulated output (4-28V, 8A)
- Battery charging supports 0, 1 or 2 Li-Ion 16.8V batteries; batteries can disconnect and reconnect at any time.
- 2 programmable overtemperature (OT) limits
- Programmable crowbar current limits
- kHz-speed perturb-and-observe agile MPPT algorithm on each solar array input; each channel with independent max current setting and automatic fallback to avoid local minima
- 8 LMx35-type temperature telemetry channels
- Fully formatted telemetry via SupMCU
- External sync clock (input or output)
- Configurable watchdog timer (WDT)
- RBF and separation switch inhibits
- Multiple units can be paralleled
- Input overvoltage shunt
- Radiation dosimeter
- CubeSat Kit-compatible footprint
- Environment:
  - Tested to NASA GEVS (14grms) levels
  - Satisfies JSC EP-WI-032 for use on ISS
  - Satisfies NASA flight safety program for use on ISS

ORDERING INFORMATION

Pumpkin P/N 710-0XXXX

Option Code	Configuration
/INN	I2C address = 0xNN (0x54 is default)

CAUTION

Electrostatic Sensitive Devices

Handle with Care

- 10-layer, 8-layer and 4-layer gold-plated blue-soldermask PCBs with ground planes for enhanced signal integrity
- Supervisor MCU programmed with Pumpkin's space-proven Salvo™ RTOS
- Mission-specific configurations:
  - OT1 & OT2 limits
  - WDT interval
  - Boot-time max battery charging currents
  - Maximum SAI input currents

CHANGELOG

Rev.	Date	Author	Comments
A	20161210	AEK	Initial release of hardware Rev A.
B	20191227	AEK	Update to reflect realities of Rev C preproduction unit.
C	20190321	AEK	Updated with details on the MPPT operation.
D	20190726	AEK	Additional updates, more data points, details on no-load/shunt operation and impact on ring bus voltage.
E	20190819	AEK	Clarified H1 & H2 pinouts, and power signals associated with them. Corrected battery connector pinouts.
F	20201101	AEK	Added studio picture, and EMI/EMF section w/1-5MHz captures.
G	20201210	AEK	Updated with complete connector pinout, illustrations of SAI and BAT connectors, added to features list.
H	20220121	AEK	Updated to reflect features of recent upgrades.
I	20230209	AEK	Updated to reflect features of recent upgrades, added more connector descriptions.

OVERVIEW

The Pumpkin Electrical Power System Module 1 (EPSM1) accepts input power from solar panels and arrays, batteries and external sources and converts it to output power at various voltage levels. Twelve versatile and efficient buck/boost switching power-converting blocks convert voltage levels at the inputs and outputs to the voltage of the internal power ring. The EPSM1 is directly compatible with the established CubeSat module form factor and its 104-pin connector. The EPSM1 is intended for use with zero, one or two dedicated, protected batteries like Pumpkin's Battery Module 2 (BM 2), and may be compatible with other battery systems.

An SEU-immune FPGA controls each GaNFET-based boost/buck block at 200kHz switching frequencies. Each buck/boost blocks has a native 80V and 8A maximum rating; a 36V maximum voltage limit is chosen for safety derating. Each block has a minimum efficiency of 97.5% over a wide range of operating currents, has a programmable current limit, and is protected against overcurrent faults. Overall power handling is a function of the thermal properties of the system that incorporates the EPSM1. Maximum current (and effectively, power) limits are imposed on each block through the connectors associated with a given block / function. The EPSM1 also includes a high-current solar array input overvoltage shunt to handle transient loads and coming-out-of-eclipse conditions.

While all twelve blocks are fundamentally identical, the EPSM1 dedicates six blocks to solar array inputs (SAIs) with MPPT functionality, three blocks (3V3, 5V0 & 12V) to regulated outputs at fixed voltages, one block to a regulated output block at a user-programmable voltage (AUX) and with ON/OFF control, and two to battery (BAT) blocks that can charge and discharge the attached batteries. SAI blocks boost their input to the ring voltage, output blocks buck the ring voltage to their output voltages, and battery blocks can boost to or buck from the ring voltage when discharging or charging the batteries, respectively. By convention, currents sourcing power into the ring are positive/'+', and currents sinking power out of the ring are negative/'-'.

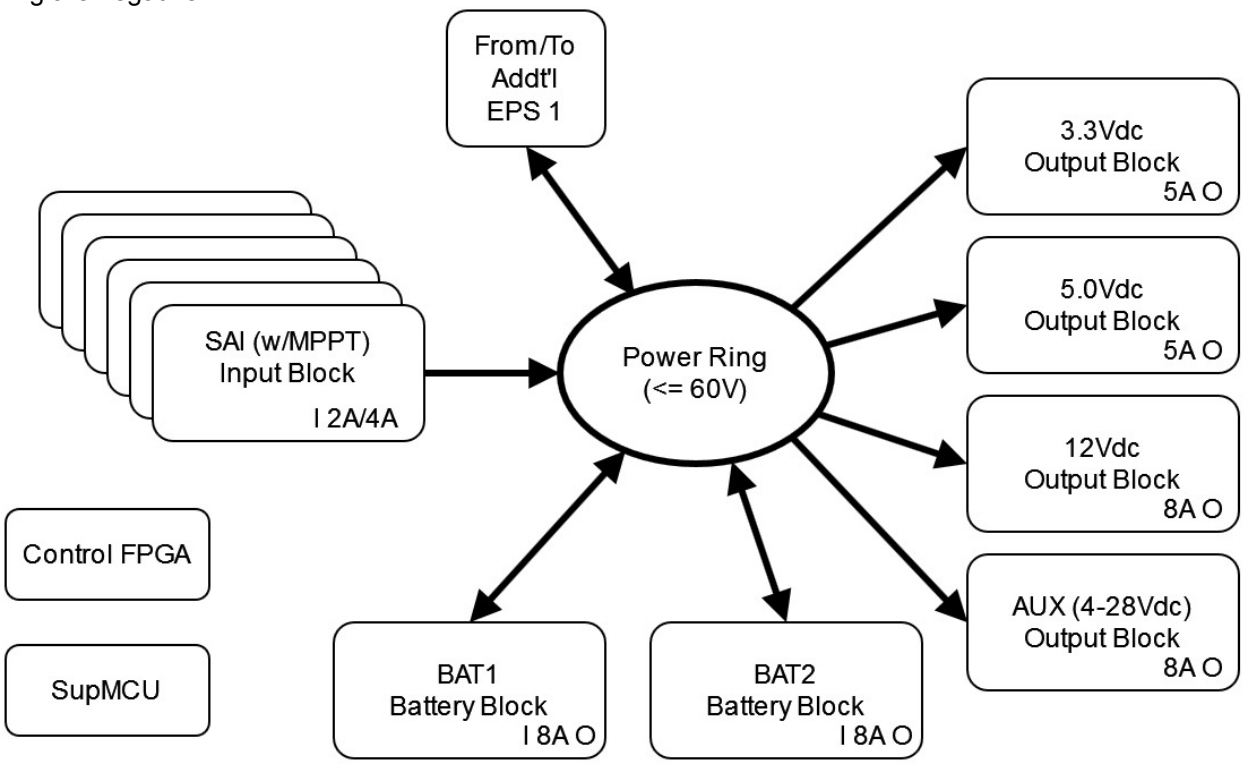


Figure 1: EPSM1 overall topology

EPSM1 input power is sourced from solar panels, external sources and batteries. The presence of any input power source of sufficient level activates the EPSM1; it manages power sources and loads automatically, assuming sufficient source power exists to serve the instantaneous loads. With input power present, the EPSM1 outputs are enabled. Three of the output blocks follow the established standard CubeSat voltage levels (regulated +3.3Vdc, regulated +5Vdc and regulated +12Vdc); the fourth output block (AUX) is nominally +28Vdc but can be reconfigured for another, lower voltage if desired. The

battery charger block(s) are input/output blocks, capable of drawing power from the batteries as needed, and automatically (re-)charge the batteries when excess SAI power is available.

The FPGA manages the power ring and all of the blocks, and implements the MPPT, battery charging power sharing and load response algorithms. A SupMCU supervisor controls the configuration of the FPGA, acquires telemetry from it, and implements additional battery charging and other higher-level functions. Control of and fully formatted telemetry from the EPSM1 are provided via SCPI over I2C through the EPSM1's SupMCU.

Solar array inputs are via discrete connectors that are limited to 2A each (SAI1-SAI4) and 4A each (SAI5-SAI6). Regulated and unregulated outputs are via the CubeSat Kit's 104-pin connector and are limited to 5A each (+3.3Vdc & +5Vdc) and 8A (+12Vdc, AUX). Battery charger connections are via dedicated, high-current connectorized harnesses limited to 8A each.

Advanced features include the ability to synchronize the switching and operating frequencies to an external clock source; to parallel multiple units for greater power handling; and to implement application-specific battery charging schemes.

OPERATIONAL DESCRIPTION

The EPSM1 is configured at the factory for a particular mix of inputs and outputs, with voltage and current settings for each block. When a minimum power is provided via an input block to the power ring, and the deployment switches are not inhibiting operation, the EPSM1's FPGA and SupMCU "go live". When sufficient power is available on the power ring, the outputs are enabled. As long as sufficient input power is present, the FPGA continuously manages all of the blocks to ensure that:

- Input blocks convert input voltage to ring voltage within their prescribed current limits
- Output blocks convert ring voltage to output voltage and deliver it to their connected loads at up to their prescribed current limits
- Input/Output blocks (i.e., the battery charger block(s)) control current into or out of the ring, based on output block current requirements and power available into the ring

The unregulated ring voltage is automatically managed by the FPGA, based on instantaneous input and output voltage requirements; the ring voltage typically varies over time and is only available to other, paralleled EPSM1 units (if present). All blocks are clocked at the same frequency, with polyphase clock phase management to minimize radiated emissions.

The EPSM1's runtime operation prioritizes power based on real-time demands, subject to the system's configurable current limits. When the SAIs can provide enough power to serve the loads, then power flows exclusively from the SAIs to the loads. If the loads exceed the instantaneous power available from the SAIs, then the batteries will provide the remaining power required by the loads. When SAI power exceeds the loads and the batteries are not fully charged, the remaining SAI power serves to (re-)charge the batteries. This all occurs automatically, at very high speeds, without any user or SupMCU intervention.

For input blocks that are configured as solar array inputs, the FPGA applies an MPPT algorithm at each input so as to maximize the power that can be drawn from the attached solar panels, while feeding the ring. Because of this, solar string input voltages and currents can be different for each SAI. The MPPT algorithm implements a perturb-and-observe control routine at kHz rates. All of the solar array inputs are simultaneously MPPT tracked at high speed. The peak power point for each of the six inputs is calculated to mW resolution with deterministic timing and is used internally by the FPGA. The FPGA also balances the power drawn from the solar array inputs when a surplus of power is available by progressively off-peak-tracking the strongest inputs. Thus, the EPSM remains highly agile to any overall system changes like dynamic shadowing (tumbling S/C), system load steps, or available power drifting from the thermal changes experienced by the solar arrays. This system's performance is markedly improved over bracketed peak power trackers (i.e., ones that periodically completely unload then re-establish the peak power point). Operation of the individual MPPTs and the system power sharing is completely transparent to the user.

Output blocks are configured for an output voltage and a maximum current; the FPGA maintains the output voltage by bucking the ring voltage through the corresponding block. Simultaneously, the current drawn from the block is monitored against a preset maximum; if an overcurrent trip is detected, the FPGA will soft-limit the output until the overcurrent condition is removed, and automatically re-enable the output.

A battery block represents the ability to both source power into the power ring (when discharging the battery), and sinking power from the ring (when charging the battery). The FPGA will automatically switch a battery block between input and output modes, and between boost and buck modes, depending on overall system power availability and loads. Each battery charger block connects to a dedicated battery, with current and voltage settings tailored to a particular battery chemistry; these charging parameters are managed over time by the SupMCU, which configures the FPGA's control of those blocks as required. The two charger blocks operate completely independently of one another.

Telemetry is available via the SupMCU's SCPI interface over I2C whenever the EPSM1's electronics are active.

CONSTRUCTION

The EPSM1 consists of three PCBs: a motherboard with the switching blocks, ring bus capacitors, SupMCU and other components, an FPGA daughterboard with the FPGA and analog interfaces, and a lid card with the overvoltage shunt, more ring bus capacitors and other components. Interface connectors are present on the motherboard and lid card. Particular attention has been paid to thermal paths while maintaining ground plane isolation from the CubeSat chassis while providing a heat path to the chassis.

MOUNTING & INSTALLATION

The EPSM1 can be installed in any module stack that is compatible with the existing CubeSat module standard. It is compatible with battery modules that plug into the stack, as well as with remote battery modules. The entire module has a nominal 90x96mm footprint and is approximately one PC/104 module (0.600" / 15.24mm) tall without any additional heatsinks. A heat spreader / heatsink module is attached to the underside to help cool the switching blocks applications.

TYPICAL USAGE

The EPSM1 is normally used in conjunction with multiple external solar panels, one or more external battery modules, and additional external power sources (e.g., ground charging supplies); the loads connected to it can draw power from regulated-voltage and unregulated-voltage power buses. The very high minimum block efficiency and the low quiescent power dissipation simplify system integration.

Mechanically / structurally, the EPSM1 should be mounted to a structure that provides a good thermal path and heatsink for the thermal standoffs, as high power levels in the EPSM1 will create waste heat.

Electrically, the interface is through the 104-pin CubeSat bus connector and through the SAI 10-pin connectors and BAT14-pin connectors. Each SAI connector has the same pinout, and serves two connected and independent solar panels. Each BAT connector has the same pinout, and matches the Pumpkin BM 2 battery module connector. A compatible battery can be connected to the EPSM1 either through the 104-pin CubeSat Kit bus connector, or through one or both of the 14-pin connectors.

In a simple, relatively low-power application, the EPSM1 will be connected to a compatible battery via the 104-pin CSK bus connector. Battery charge/discharge currents and output discharge currents will be limited by the pin ratings of the CSK bus connector.

In more sophisticated applications that require higher power levels, the two identical 14-pin BAT block connectors enable a wide variety of useful configurations. For example, one BAT connector can be used for relatively high-rate (8A) charging and discharging of a remotely connected battery, while the second BAT connector can be used for a smaller battery of different capacity.

Only 16.8V 4S2P Li-Ion batteries are supported. Only one battery (BAT1) can have its unregulated battery voltage exposed on the 104-pin CSK bus.

COMMAND & TELEMETRY INTERFACE

A Pumpkin SupMCU provides a command and telemetry interface to the EPSM1, via SCPI over I2C. Commands and telemetry are both EPSM1-specific and general to SupMCUs. Most of the telemetry is passed through the SupMCU from the gas gauge FPGA, and includes comprehensive voltage, current and temperature information on the blocks, as well as overall system status.

The I2C address of the EPSM1 is configured in software. Multiple EPSM1s can be accommodated on a single I2C bus thusly.

The I2C bus is extended through the EPSM1 such that I2C traffic destined for up to two connected batteries will pass through the EPSM1 to reach the batteries; standard BM 2 I2C addresses are used.

DEBUGGING/PROGRAMMING INTERFACE

Three connectors are provided for SupMCU (re-)programming, a debug terminal to the SupMCU, and an interface to the FPGA. These are typically only used at the factory.

ABSOLUTE MAXIMUM RATINGS

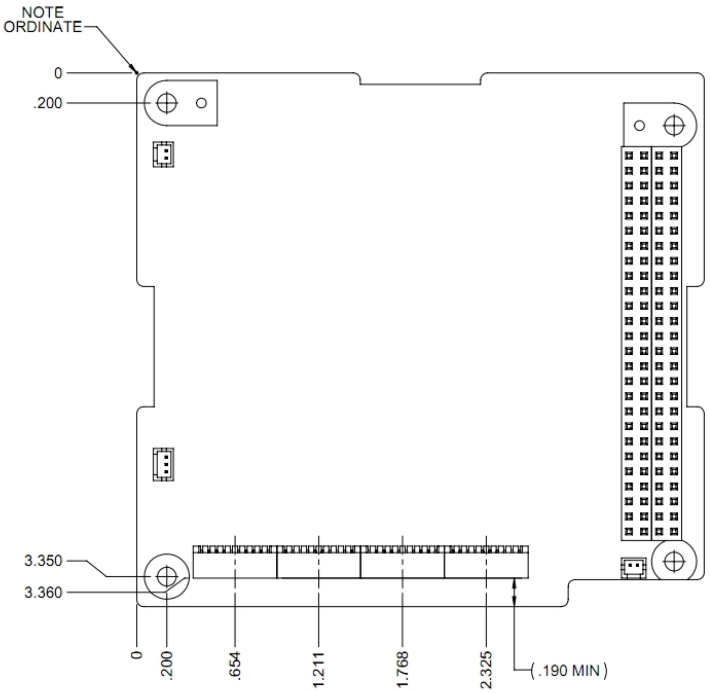
All voltages relative to system **GND**.

Parameter	Conditions / Notes	Symbol	Value	Units
Operating temperature		T_{OP}	-40 to +85	ºC
Voltage on **–RESET**, **OFF_VCC**, **SCL_SYS**, **SDA_SYS**, **SYNC**			-0.3 to +6.0	V
Voltage on any SAI POS input			-0.3 to +55	V
Voltage on any SAI TLM input			+3.3	V
Voltage on any BAT V+ input			-0.3 to +16.8	V
Voltage on any BAT logic input			-0.3 to +3.6	V
Frequency of clock input on **SYNC**			60	MHz
Block current	SAI1, SAI2, SAI3, SAI4		+2100	mA
	SAI5, SAI6		+4200	
	Battery block (charge)		-8400	
	Battery block (discharge)		+8400	
	3.3V block		-5250	
	5V block		-5250	
	12V block (includes current from 5V & 3.3V blocks)		-8400	
	AUX block		-8400	
Overvoltage shunt energy	50C rise in shunt		5000	mJ

PHYSICAL CHARACTERISTICS

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Mass	Aluminum standoffs, no heat spreader			230		g
Length				96		mm
Width				90		mm
Height				15.24		mm

SIMPLIFIED MECHANICAL LAYOUT [1]



[1] Dimensions in inches [mm].

ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes		Symbol	Min	Typ	Max	Units
Operating power consumption	Deployment switches not inhibited; no commands or telemetry active over I2C; all LEDs off,		P_{OP_XXX}	TBD	2000	TBD	mW
Block efficiency, at stated voltage and power input, buck / down mode [2]	10V	2.7W			96.5		%
		10.0W			97.3		
		18.6W			96.3		
	15V	6.0W			96.7		
		22.6W			97.3		
		32.8W			96.8		
	20V	10.0W			96.7		
		40.2W			96.5		
		74.4W			96.3		
	25V	16.9W			96.8		
		62.7W			97.3		
		116.1W			96.0		
	30V	24.3W			96.9		
		90.7W			97.2		
		130.5W			96.7		
Block switching frequency					250		kHz
Block duty cycle				5		95	%
Block output voltage regulation					1		%
Output noise (3.3V output)	20MHz bandwidth	no load				25	mV_{RMS}
		2A load				85	
Peak inrush current	On solar array inputs					+1000	mA
	On battery inputs					+15	A
Solar array input voltage	Input to MPPT-equipped block; SAI1-SAI6; normal operating conditions			8		28	V
Solar array input overvoltage shunt turn-on voltage	Maximum shunt energy must not be exceeded			62	65	72	V
Solar array input current	Input to MPPT-equipped block; SAI1-SAI4					+2000	mA
	Input to MPPT-equipped block; SAI5-SAI6					+4000	mA
Battery charging voltage					16.4		V
Battery current	Discharging			+10		+8000	mA
	Charging			-10		-8000	mA
Block output voltage	AUX block			4.0		28	V
Block output current				-10		-8000	mA
Supervisor MCU internal clock frequency	Base frequency, can be multiplied by onboard PLL		f_{CLK_MCU}	29.5			MHz
-RESET signal validity	**-RESET** driven by external source			0		0.5	V

[2] Overall system efficiency is given by input-to-output power path, i.e. by the sum of the products of the input and output block efficiencies. Does not include system-wide power operating power consumption.

ELECTRICAL CHARACTERISTICS (cont'd)

(T = 25ºC, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes		Symbol	Min	Typ	Max	Units
Voltage at inhibit switch pin 1	Switch open	J145 (RBF)		5		9	V
		J149 (Sep 1)		3.1		3.5	
		J152 (Sep 2)		3.1		3.5	
	Switch closed	All		0		0.1	V
Current through inhibit switch	Switch closed	All		500		2500	µA

I2C CHARACTERISTICS

Parameter	Conditions / Notes		Min	Typ	Max	Units
I2C address	7-bit I2C address	default		0x54		
		via option /INN		0xNN		
I2C clock speed					400	kHz
I2C pull-up resistors	No pull-up resistors are fitted to **SCL_SYS** or **SDA_SYS**			∞		Ω

SOLAR PANEL CONNECTOR PIN DESCRIPTIONS

Each solar panel connects to its associated EPSM1 input block via 5 pins on a dedicated connector; 4 ten-pin connectors are provided to connect SAI1 & SAI2 (**J141**), SAI3 & SAI4 (**J142**), SAI5 (**J143**) & SAI6 (**J144**).[3] Each connector maps two independent solar arrays to their corresponding independent input blocks. Unconnected telemetry signals must be grounded -- they must not be left floating. Each connector is pinned out as shown below:

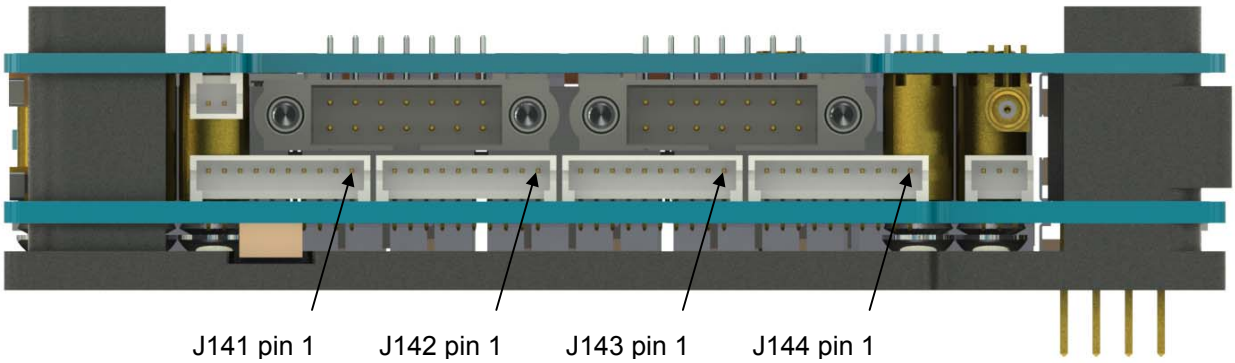


Figure 2: View into EPSM1 showing SAI connectors

Name	Pin	I/O	Description
SA_POS_n	1 2	–	Solar array positive for solar array input **n**.
SA_TLM_n	3	I	Solar array telemetry for solar array input **n**. By convention, this is the output terminal of an LM335-class absolute Kelvin analog temperature sensor. The maximum voltage allowed on this signal is +3.3Vdc; must be connected to **SA_RTN_n** when not in use.
SA_RTN_n	4 5	–	Solar array negative for solar array input **n**. Also to be connected to the ground terminal of a remote LM335 temperature sensor.
SA_POS_n+1	6 7	–	Solar array positive for solar array input **n+1**.
SA_TLM_n+1	8	I	Solar array telemetry for solar array input **n+1**. By convention, this is the output terminal of an LM335-class absolute Kelvin analog temperature sensor. The maximum voltage allowed on this signal is +3.3Vdc; must be connected to **SA_RTN_n+1** when not in use.
SA_RTN_n+1	9 10	–	Solar array negative for solar array input **n+1**. Also to be connected to the ground terminal of a remote LM335 temperature sensor.

The SAI signals are distributed across the **J141-J144** connectors as shown below. Each of the four SAIs with lower current ratings (SAI1-SAI4) is pinned out to five of the pins of the associated connector. The two higher-current SAIs (SAI5 & SAI6) each get their own, dedicated ten-pin connector.

Connector	Pins	SAI	Description
J141	1-5	1	SAI1 and SAI2 are both pinned out on **J141**.
	6-10	2	
J142	1-5	3	SAI3 and SAI4 are both pinned out on **J142**.
	6-10	4	
J143	1-10	5	SAI5 is pinned out exclusively on **J143**.
J144	1-10	6	SAI6 is pinned out exclusively on **J144**.

Each pin is rated at up to 1A @ 25C. The mating connector for **J141-J144** is the Hirose P/N DF13-10S-1.25C; 26-30AWG wire is to be used, with crimp-type pin connectors.

[3] The EPSM1 does not use Battery Charge Regulator (BCR) nomenclature; each solar array input (SAI) block with MPPT maximizes power input into the EPSM1 ring, and has nothing to do with battery charge regulation per se. The (independent) battery blocks implement battery charging and discharging.

BATTERY BLOCK CONNECTOR PIN DESCRIPTIONS

Each BAT block on the EPSM1 has a dedicated connector. The two identical 14-pin connectors **J147** & **J148** match the pinout of the Pumpkin BM 2 battery module connectors. These connectors provide a high-current charge/discharge path for a remotely-connected battery, as well as some control and telemetry signals to and from the connected battery. Their pinout is shown below:

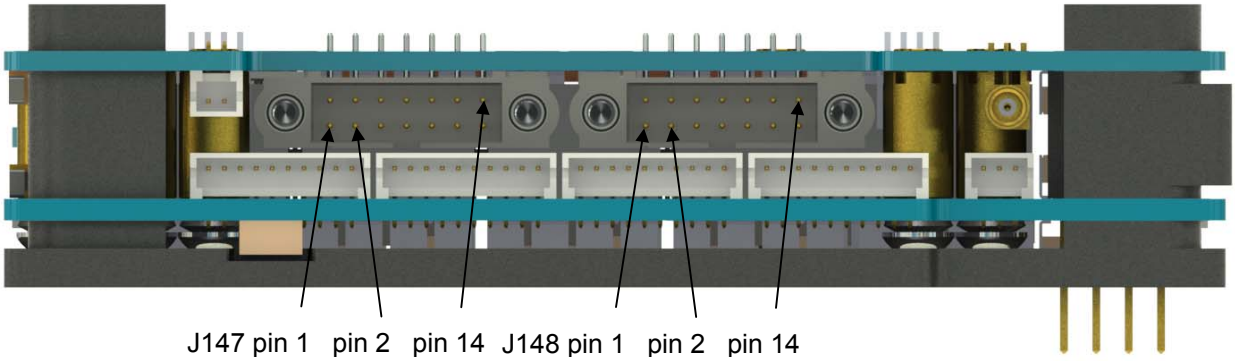


Figure 3: View into EPSM1 showing BAT connectors

Name	Pin	I/O	Description
V+	1 2 3 4 5	–	Battery positive terminal.
V-	8 9 10 11 12	–	Battery negative terminal. Connected to system (power) ground **PGND**.
OFF_VCC	6	O	From the CSK bus **OFF_VCC** signal.
-RESET	13	O	From the CSK bus **-RESET** signal.
SDA_SYS	7	O/I	From/to the CSK bus **SDA_SYS** signal.
SCL_SYS	14	O	From/to the CSK bus **SCL_SYS** signal.

Each pin is rated at up to 3A @ 25C. A pair of screw terminals is used to secure each connector in place. The mating connector is Harwin P/N M80-4801442; 22AWG wire is to be used, with crimp-type pin connectors.

The I2C interface is used to communicate with the Pumpkin BM 2's SupMCU via SCPI. **–RESET** and **OFF_VCC** are used by the BM 2 to ensure an orderly power-on, etc.

When an I/O block is not connected to a BM 2 battery and is instead repurposed,[4] users will typically connect only the **V+** and **V-** terminals, and leave the remaining four terminals unconnected.

IN-CIRCUIT DEBUGGING PIN DESCRIPTIONS

The Microchip® ICD®-compatible debugging/ programming connector **J5** is implemented with a standard 6-pin Pumpkin PIC24 FPC connector. It is designed to mate to a Pumpkin JFPC-PIC24 debugging adapter via a 6-terminal flexible printed circuit (cable). This in turn can be connected to various Microchip in-circuit debuggers and programmers.

Name	Pin	I/O	Description
	J5.1	–	Unused.
PGEC	**J5.2**	I/O	**PGEC1** – clock signal for in-circuit debugging.

[4] Repurposing requires alternate FPGA programming from the factory.

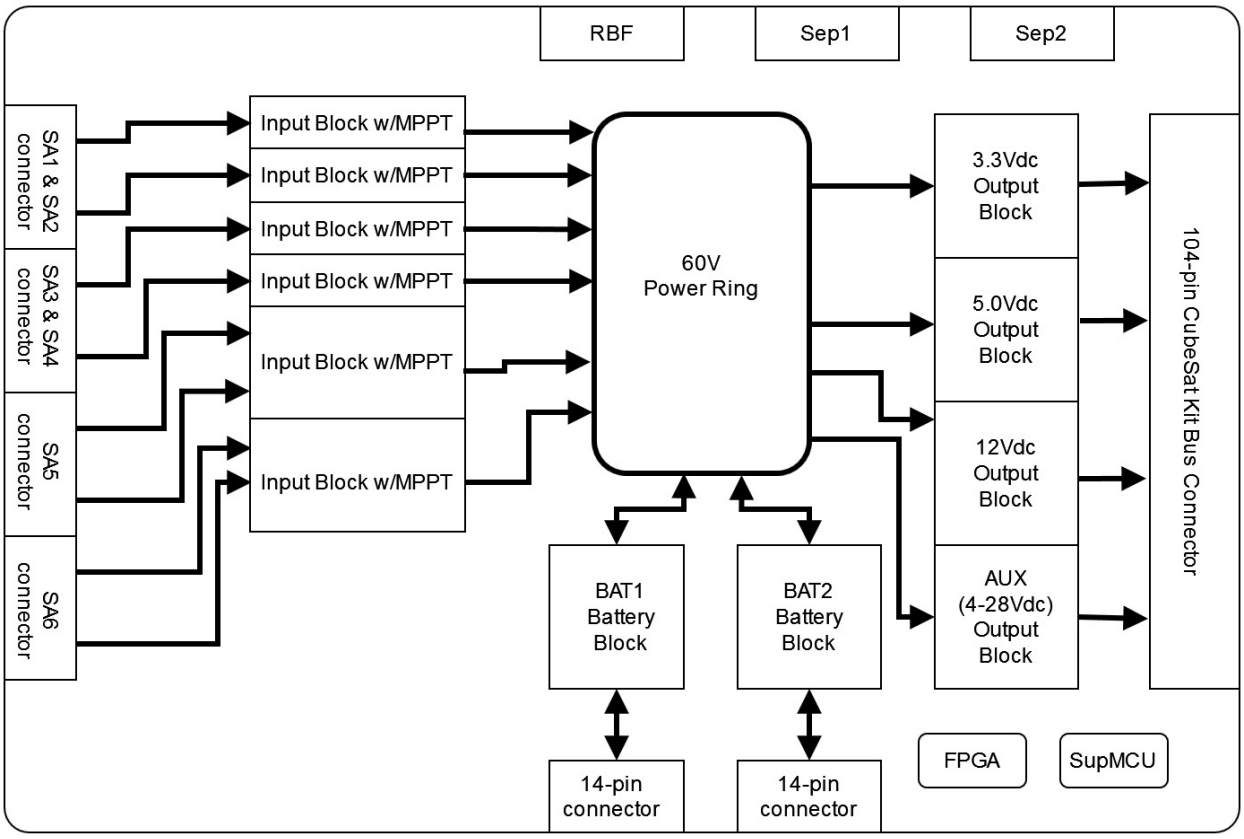
PGED	**J5.3**	I/O	**PGED1** – data signal for in-circuit debugging.
DGND	**J5.4**	–	Digital ground.
VCC	**J5.5**	–	Supervisor MCU power.
-MCLR	**J5.6**	I	Supervisor MCU's reset.

DEBUGGING ADAPTER PIN DESCRIPTIONS

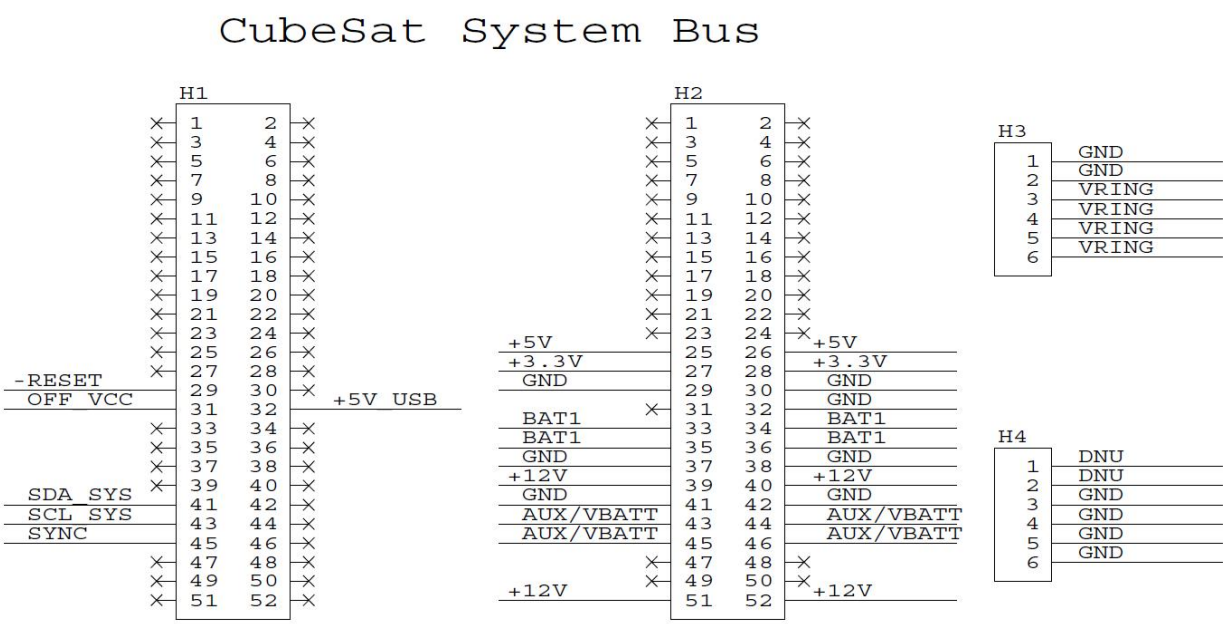
The Pumpkin USB Debugging Adapter-compatible debugging connector **J6** is implemented with a standard 4-pin Pumpkin USB Debug FPC connector. It is designed to mate to a Pumpkin USB Debugging Adapter via a 4-terminal flexible printed circuit (cable). The serial interface is configured as 115200,N,8,1.

Name	Pin	I/O	Description
VCC	**J6.1**	–	Supervisor MCU power. When used with the BM 2, users must ensure that this voltage from the Pumpkin USB Debug Adapter is set to 3.3V, or disconnected (preferred).
DGND	**J6.2**	–	Digital ground.
TXD	**J6.3**	O	Asynchronous serial data out of the Supervisor MCU.
RXD	**J6.4**	I	Asynchronous serial data into the Supervisor MCU.

BLOCK DIAGRAM



CubeSat Kit Bus PIN DESCRIPTIONS



CubeSat Kit Bus PIN DESCRIPTIONS – I/O

Name	Pin	I/O	Description
IO.0	H1.24		Not connected.
IO.1	H1.23		Not connected.
IO.2	H1.22		Not connected.
IO.3	H1.21		Not connected.
IO.4	H1.20		Not connected.
IO.5	H1.19		Not connected.
IO.6	H1.18		Not connected.
IO.7	H1.17		Not connected.
IO.8	H1.16		Not connected.
IO.9	H1.15		Not connected.
IO.10	H1.14		Not connected.
IO.11	H1.13		Not connected.
IO.12	H1.12		Not connected.
IO.13	H1.11		Not connected.
IO.14	H1.10		Not connected.
IO.15	H1.9		Not connected.
IO.16	H1.8		Not connected.
IO.17	H1.7		Not connected.
IO.18	H1.6		Not connected.
IO.19	H1.5		Not connected.
IO.20	H1.4		Not connected.
IO.21	H1.3		Not connected.
IO.22	H1.2		Not connected.
IO.23	H1.1		Not connected.
IO.24	H2.24		Not connected.
IO.25	H2.23		Not connected.
IO.26	H2.22		Not connected.
IO.27	H2.21		Not connected.
IO.28	H2.20		Not connected.
IO.29	H2.19		Not connected.
IO.30	H2.18		Not connected.
IO.31	H2.17		Not connected.

IO.32	H2.16		Not connected.
IO.33	H2.15		Not connected.
IO.34	H2.14		Not connected.
IO.35	H2.13		Not connected.
IO.36	H2.12		Not connected.
IO.37	H2.11		Not connected.
IO.38	H2.10		Not connected.
IO.39	H2.9		Not connected.
IO.40	H2.8		Not connected.
IO.41	H2.7		Not connected.
IO.42	H2.6		Not connected.
IO.43	H2.5		Not connected.
IO.44	H2.4		Not connected.
IO.45	H2.3		Not connected.
IO.46	H2.2		Not connected.
IO.47	H2.1		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	Description
VREF0	H1.26		Not connected.
VREF1	H1.28		Not connected.
VREF2	H1.30		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	Description
RSVD0	H1.44		Not connected.
RSVD1	H1.45	I/O	**SYNC** signal to/from EPSM1 and connected battery SupMCUs.

CubeSat Kit Bus PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	Description
SDA_SYS	H1.41	I/O	I2C data. To/from EPSM1 and connected battery SupMCUs (all I2C slave devices) via I2C isolators. Typically from/to the primary host (an I2C master).
SCL_SYS	H1.43	I	I2C clock. To EPSM1 and connected battery SupMCUs (all I2C slave devices) via I2C isolators. Typically from the primary host (an I2C master).

CubeSat Kit Bus PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	Description
-FAULT	H1.25		Not connected.
SENSE	H1.27		Not connected.
-RESET	H1.29	I/O	Input to EPSM1 and connected battery reset supervisors. *An active signal (0Vdc) on this input will reset the EPSM1's and connected battery SupMCUs if the SupMCU is configured to respond to -RESET..*
OFF_VCC	H1.31	I	Input to latchup-prevention overcurrent switch. *An active signal (+5Vdc) on this input will disable **+5V_SYS** power to the EPSM1 and connected batteries.*
PPS	H1.46		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – RBF and Separation Switches

Name	Pin	I/O	Description
BAT1_POS (S0)	H2.33 H2.34		BAT 1 positive terminal (source or sink). These terminals are provided only for compatibility with CubeSat-class batteries that have traditionally been connected to these terminals due to historical reasons. *Exercise caution when utilizing the EPSM1 with batteries that connect to the system via H2.*
BAT1_POS (S1)	H2.35 H2.36		
GND (S1)	H2.37 H2.38		(Power) ground.

+12V (S3)	H2.39 H2.40		+12V regulated output.
GND (S4)	H2.41 H2.42		(Power) ground.
AUX/VBATT (S5)	H2.43 H2.44		Auxiliary regulated output. See description below. *Exercise caution when utilizing the EPSM1 with modules that draw power from VBATT (traditionally 8.4V or 12.6V).*

CubeSat Kit Bus PIN DESCRIPTIONS – Power

Name	Pin	I/O	Description
AUX/VBATT (VBATT)	H2.45 H2.46	–	Auxiliary regulated output. To disable AUX, remove **R88.** To connect to BAT 1 instead, disable AUX and fit **R89** & **R251**. To connect to BAT 2 instead, disable AUX and fit **R90** & **R252**. *Exercise caution when utilizing the EPSM1 with modules that draw power from VBATT (traditionally 8.4V or 12.6V).*
+5V_USB	H1.32	–	+5V USB power. From USB host.
+5V (+5V_SYS)	H2.25 H2.26	–	+5V regulated output.
PWR_MHX	H1.33		Not connected.
VBACKUP	H1.42		Not connected.
+3.3V (VCC_SYS)	H2.27 H2.28	–	+3.3V regulated output.
AGND	H2.31		Not connected.
GND	H2.29 H2.30 H2.32	–	(Power) ground.

CubeSat Kit Bus PIN DESCRIPTIONS – Transceiver Interface

Name	Pin	I/O	Description
-RST_MHX	H1.34		Not connected.
-CTS_MHX	H1.35		Not connected.
-RTS_MHX	H1.36		Not connected.
-DSR_MHX	H1.37		Not connected.
-DTR_MHX	H1.38		Not connected.
TXD_MHX	H1.39		Not connected.
RXD_MHX	H1.40		Not connected.

CubeSat Kit Bus PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	Description
USER0	H1.47		Not connected.
USER1	H1.48		Not connected.
USER2	H1.49		Not connected.
USER3	H1.50		Not connected.
USER4	H1.51		Not connected.
USER5	H1.52		Not connected.
USER6	H2.47		Not connected.
USER7	H2.48		Not connected.
USER8	H2.49		Not connected.
USER9	H2.50		Not connected.
+12V (+12V_SYS)	H2.51 H2.52	–	+12V regulated output. To isolate **USER** pins, remove **R129** and **R249 (USER10)** and **R130** and **R250 (USER11)**.

CubeSat Kit Bus PIN DESCRIPTIONS – EPSM Expansion

Name	Pin	I/O	Description
GND	H3.1	–	(Power) ground.

	H3.2		
VRING	H3.3 H3.4 H3.5 H3.6	–	Reserved. Do not connect anything to these pins.
DNU	H4.1 H4.2	–	Reserved. Do not connect anything to these pins.
GND	H4.3 H4.4 H5.5 H6.6	–	(Power) ground.

Overtemperature Protection

The EPSM1's SupMCU actively monitors three temperature points within the EPSM1 against overtemperature (OT) conditions and compares them against two programmable limit values, OT1 and OT2. OT1 is normally 15C or so below OT2.

OT conditions can arise from a continuously high ring bus voltage (in which case the OV clamp is active and shunting, creating heat), a high thermal load in the solar array inputs, a high thermal load in an output regulator and/or a high thermal load in a battery block. When any of the monitored temperatures exceeds a preprogrammed limit, the SupMCU will seek to reduce the overall system temperature by:

- When the OT1 (load shedding) trip point is exceed, the AUX output is automatically disabled, and will be automatically re-enabled once the temperatures have dropped by the hysteresis amount.
- When the OT2 (system overheat) trip point is exceeded, the EPSM1 reboots, thereby effecting a WDT-style reboot of the entire system (including the attached spacecraft).

The SupMCU is not able to reduce temperatures by throttling power delivered from the 12V, 5V or 3.3V blocks.

EMI/EMF

A typical capture of the frequency content of the EPSM's outputs is shown below.

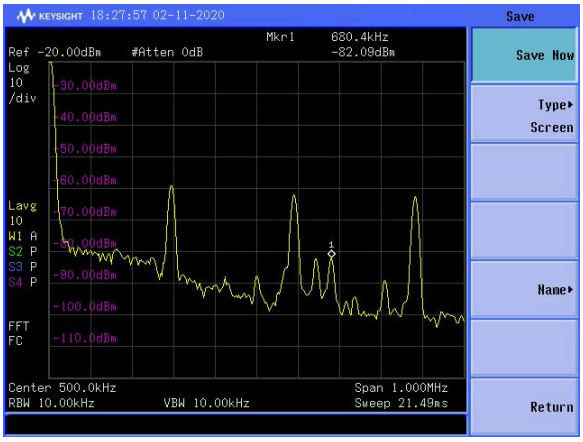


Figure 4: 1MHz spectrum of 3.3V output when powered via SAI1-SAI6

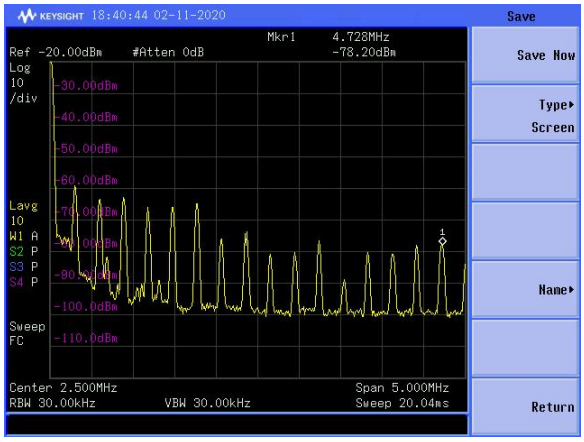


Figure 5: 5MHz spectrum of 3.3V output when powered via SAI1-SAI6

The 250kHz switching frequency is readily apparent.

Overvoltage Shunt

An active overvoltage (OV) shunt with an integrated power resistor is located on the underside of the EPSM1's lid card. It is used to prevent the ring bus voltage from reaching a level that can damage the EPSM1's electronics. In most operational scenarios, the ring voltage will remain well below the shunt clamping voltage. "Unloading" a heavily loaded output will usually result in a small but very short clamping action by the OV shunt, and this is part of normal operation and does not affect the EPSM1's runtime or lifetime performance.

However, excessively high SAI (input) voltages and battery voltages over 16.4V will result in the OV shunt actively clamping the OV condition on the ring bus. The shunt and its power resistor have a finite thermal capacity, and the input power to the shunt is limited only by the source (one or more solar array inputs, and/or battery inputs). Therefore, the user must ensure that the OV shunt operates within its Safe Operating Area (SOA) as a function of the input voltages to the EPSM1 and the loads applied to it. For low SAI voltages (<40Vdc) and battery voltages below the float voltage, this is generally not an issue. For higher voltages, care must be taken to ensure that the OV shunt's SOA is observed. Note that an attached solar array coming out of eclipse will typically generate higher-than-normal voltages while the cells are still cold; during this warm-up period, the OV shunt may actively dumping energy into its shunt resistor, depending on the voltage(s) applied to the EPSM1's SAIs.

The OV shunt can be configured to use an external, higher-power resistor for those configurations where SOA-violating excursions into the OV shunt's active region are expected. Contact the factory for more information.

Battery Charging

Each EPSM1 battery charger supports 4S2P (16.8V) Li-Ion battery configurations. The default battery charger characteristics are matched to the Pumpkin BM 2 battery module and its cell chemistry, and are outlined below. Only 4S (16.8V) battery configurations are supported, as the fixed current limit of 8A per block results in 3S and 2S battery configurations being unable to deliver adequate power, in relation to the system's output capabilities.

Configuration & chemistry	Mode	Initial CC current (A)	Max CC current (A)	CC to CV transition current (A)	Float voltage (V)	Trickle / 0V charging supported?
4SNP, Li-Ion	CC/CV	6.0	6.0	1	16.4	yes

The high currents available via the EPSM1 battery charger block enable rapid charging of compatible batteries. For example, the 100Wh Pumpkin BM 2 battery module in its 4S2P configuration can be fully recharged via the EPSM1 in roughly one half hour.

Since the EPSM1 prioritizes SAI power to the loads, its is safe to operate with a high maximum battery charging current at all times; the batteries will not "steal" power from the loads. Only if/when SAI power is greater than the loads, will excess SAI power be routed to the batteries for battery charging, as required. Maximum battery charging current is an NVM parameter that can be changed by the user..

It is important to note that the EPSM1 battery charger does not implement any battery safety functions, beyond the maximum current and voltage applied to the battery. Overvoltage, overcurrent, overtemperature and other battery protections must be implemented locally within the battery module, as is the case with the Pumpkin BM2 battery.

Additional charging configurations (e.g., for alternate battery configurations, chemistries and/or capacities) may be possible – please contact the factory.

Module Inhibits

The EPSM1 includes three independent system-level inhibits. Remove-Before-Flight (RBF) and Separation (Sep) switch functionality are available through these inhibits. The three inhibits can be used independently or logically combined with logical AND and OR operations via RBF and Sep switch electrical wiring schemes.

Each inhibit is activated by shorting two pins of its associated connector together; this is typically done by an external SPST switch or equivalent. Little to no current flows within the inhibit circuits. When an inhibit connector is left unpopulated or unconnected, the corresponding inhibit function is inactive. When the pins on an inhibit connector are connected together, the corresponding inhibit is enabled. The RBF connector is implemented via a 3-pin Hirose DF13-series header, and the Sep connectors are implemented via 2-pin Hirose DF13-series headers.

N.B. *Each inhibit must be connected to an independent switch without any connections to any other inhibit switches, or to any other EPSM1 signals, including (power) ground,* **GND**.

There are no sequencing requirements for RBF and Sep inhibits.

Name	Connector	Function	Description
RBF	**J145** pins 1&2 or 2&3	RBF Inhibit	When active, disconnects all inputs from the EPSM1.
Sep1	**J149** pins 1&2	Separation Inhibit	Not operational.
Sep 2	**J152** pins 1&2		When active, disconnects output blocks from the power ring, i.e., power cannot leave the ring.

Reset Behavior

The EPSM1 has its own dedicated power-on-reset (POR) controller. The EPSM1's **–RESET** input is normally ignored.

System power-up with source power (SAI or BAT) available and no inhibits is within ca. 8s.

Telemetry

The EPSM1 provides a wide range of telemetry. Telemetry is acquired by making SCPI telemetry request commands to the EPSM1's SupMCU.

External Oscillator into SupMCU[5]

The EPSM1's SupMCU operates with an internal 15.9MHz oscillator. For applications that wish to synchronize the SupMCU's clock and the FPGA's clock with an external source, the SupMCU can be configured to run from an externally-provided oscillator applied to its **SYNC** input.

If the external oscillator signal fails, the SupMCU will automatically switchover to its internal 15.9MHz oscillator.

If/when providing an external oscillator at a frequency other than 15.9MHz, the SupMCU must be commanded with the new operating frequency, so that it can reconfigure peripherals that are dependent on particular clock speeds (e.g., UARTs).

The external oscillator in function is disabled when the oscillator out function is selected.

External Oscillator out of SupMCU[6]

The EPSM1 can output an oscillator signal on its **SYNC** output. This signal can be used to synchronize to other SupMCUs, or to derive information re the EPSM1's SupMCU operation.

The oscillator output is the SupMCU's internal clock, divided by a commandable power-of-2. This oscillator output can be enabled, disabled and the resultant frequency changed via SCPI commands.

The oscillator out function is disabled when the external oscillator in function is selected.

[5] Future software enhancement.
[6] Future software enhancement.

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